PCI CD

PCI Bus Configurable DMA Interface
Addendum for

32-bit Parallel Interface

008-01132-02

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Overview

The PCI Bus Configurable DMA Interface (PCI CD) is a single-slot, 16-bit parallel input/output interface for PCI Bus-based computer systems. It is designed for continuous input or output between a user device and PCI Bus host memory. This interface is typically used to move data to or from an PCI Bus host computer to devices such as scanners, plotters, imaging devices, or research prototypes. The PCI CD uses a simple synchronous protocol for transferring data.

This addendum describes an alternate parallel protocol that acquires and outputs synchronous 32-bit data, without handshaking. Data can be output using either an internal or a external clock. There are 35 possible input signals: 32 data bits, a clock in and a clock out, and one additional signal that can be configured using the function register described below. By default, input is collected on each rising clock edge, and a clock signal is output when data is output. Both input and output can be configured differently using the function register.

For complete information on using the PCI Bus Configurable DMA Interface, see the *PCI CD User's Guide* (EDT part number 008-00965), for which you can contact Engineering Design Team, Inc.

Included Files

In addition to the files shipped with the PCI Bus Configurable DMA Interface, the following files are shipped with the 32-bit parallel protocol:

`pcd32.bit`
: Firmware for the Xilinx gate array that implements the 32-bit parallel protocol.

Function Register

Size 8-bit

I/O read-write

Address 0x02

Comments Allows you to:

- output a counter,
- delete words composed of all zeroes from the data stream,
- change the purpose of the optional input signal, and
- change the frequency of the internally generated output clock.

Bit	PCD_	Description
D0	SELCNT	When asserted, outputs 32-bit counter, starting at 0 and counting to 2^{32}-1, then returning to 0 and starting again.
D1	ENDELZ	When asserted, deletes all-zero words from incoming data stream.
D2–3	IOP0, IOP1	Sets the function of the optional input signal according to the following: **IOP0 IOP1** 0 0 not used 0 1 Optional input is external clock input. 1 0 tristate outputs: When optional input is high, optional input disables the outputs. 1 1 When optional input is high, data is sampled on positive clock edge; when optional input is low, data is ignored on positive clock edge.
D4–7	Internal clock select bits 0–3	Divides the frequency of the internally generated output clock by 2^n where n is from 0 to 15, the value of these bits, as follows: **Value Frequency** 0 10 MHz 1 5 MHz 2 2.5 MHz ... F 305 Hz

Connector Pinout

The PCI CD board uses a high-density 80-pin I/O connector, AMP part number 749111-7, with a straight-shielded backshell (AMP P/N 749196-1) or right angle backshell (AMP P/N 749205-1).

The following pinout diagram describes the connection from the PCI CD board to the cable.

NOTE Do not connect your own circuits to the unused pins, as they may be internally connected to the PCI CD.

MIT J5	MIT J4	EDT P3	Signal
		1	Ground
		2	Ground
	10	3	Data4+
	9	4	Data4–
	12	5	Data5+
	11	6	Data5–
	14	7	Data6+
	13	8	Data6–
	16	9	Data7+
	15	10	Data7–
	26	11	Data12+
	25	12	Data12–
	28	13	Data13+
	27	14	Data13–
	30	15	Data14+
	29	16	Data14–
	32	17	Data15+
	31	18	Data15–
4		19	Clock In+
		20	+5V
10		21	Optional Input+
16		22	Clock out+
		23	Ground
40		24	Data20+
39		25	Data20–
38		26	Data21+
37		27	Data21–
36		28	Data22+
35		29	Data22–
34		30	Data23+
33		31	Data23–
24		32	Data28+
23		33	Data28–
22		34	Data29+
21		35	Data29–
20		36	Data30+
19		37	Data30–
18		38	Data31+
17		39	Data31–
		40	Ground

MIT J5	MIT J4	EDT P3	Signal
		41	Ground
		42	Ground
	2	43	Data0+
	1	44	Data0–
	4	45	Data1+
	3	46	Data1–
	6	47	Data2+
	5	48	Data2–
	8	49	Data3+
	7	50	Data3–
	18	51	Data8+
	17	52	Data8–
	20	53	Data9+
	19	54	Data9–
	22	55	Data10+
	21	56	Data10–
	24	57	Data11+
	23	58	Data11–
3		59	Clock In–
		60	+5V
9		61	Optional Input–
15		62	Clock out–
		63	Ground
	34	64	Data16+
	33	65	Data16–
	36	66	Data17+
	35	67	Data17–
	38	68	Data18+
	37	69	Data18–
	40	70	Data19+
	39	71	Data19–
32		72	Data24+
31		73	Data24–
30		74	Data25+
29		75	Data25–
28		76	Data26+
27		77	Data26–
26		78	Data27+
25		79	Data27–
		80	Ground