edt
a HEICO company

Addendum

Firmware Guide for Camera Link Products

for use with EDT Camera Link framegrabbers, extenders, and recorders

Doc. 008-01857-06
Rev. 2011 April 02

Engineering Design Team (EDT), Inc.
3423 NE John Olsen Ave
Hillsboro, OR 97124
p 503-690-1234 / 800-435-4320
f 503-690-1243
www.edt.com

Terms of Use Agreement

Definitions. This agreement, between Engineering Design Team, Inc. ("Seller") and the user or distributor ("Buyer"), covers the use and distribution of the following items provided by Seller: a) the binary and all provided source code for any and all device drivers, software libraries, utilities, and example applications (collectively, "Software"); b) the binary and all provided source code for any and all configurable or programmable devices (collectively, "Firmware"); and c) the computer boards and all other physical components (collectively, "Hardware"). Software, Firmware, and Hardware are collectively referred to as "Products." This agreement also covers Seller's published Limited Warranty ("Warranty") and all other published manuals and product information in physical, electronic, or any other form ("Documentation").

License. Seller grants Buyer the right to use or distribute Seller's Software and Firmware Products solely to enable Seller's Hardware Products. Seller's Software and Firmware must be used on the same computer as Seller's Hardware. Seller's Products and Documentation are furnished under, and may be used only in accordance with, the terms of this agreement. By using or distributing Seller's Products and Documentation, Buyer agrees to the terms of this agreement, as well as any additional agreements (such as a nondisclosure agreement) between Buyer and Seller.

Export Restrictions. Buyer will not permit Seller's Software, Firmware, or Hardware to be sent to, or used in, any other country except in compliance with applicable U.S. laws and regulations. For clarification or advice on such laws and regulations, Buyer should contact: U.S. Department of Commerce, Export Division, Washington, D.C., 20230, U.S.A.

Limitation of Rights. Seller grants Buyer a royalty-free right to modify, reproduce, and distribute executable files using the Seller's Software and Firmware, provided that: a) the source code and executable files will be used only with Seller's Hardware; b) Buyer agrees to indemnify, hold harmless, and defend Seller from and against any claims or lawsuits, including attorneys' fees, that arise or result from the use or distribution of Buyer's products containing Seller's Products. Seller's Hardware may not be copied or recreated in any form or by any means without Seller's express written consent.

No Liability for Consequential Damages. In no event will Seller, its directors, officers, employees, or agents be liable to Buyer for any consequential, incidental, or indirect damages (including damages for business interruptions, loss of business profits or information, and the like) arising out of the use or inability to use the Products, even if Seller has been advised of the possibility of such damages. Because some jurisdictions do not allow the exclusion or limitation of liability for consequential or incidental damages, the above limitations may not apply to Buyer. Seller's liability to Buyer for actual damages for any cause whatsoever, and regardless of the form of the action (whether in contract, product liability, tort including negligence, or otherwise) will be limited to fifty U.S. dollars ($50.00).

Limited Hardware Warranty. Seller warrants that the Hardware it manufactures and sells shall be free of defects in materials and workmanship for a period of 12 months from date of shipment to initial Buyer. This warranty does not apply to any product that is misused, abused, repaired, or otherwise modified by Buyer or others. Seller's sole obligation for breach of this warranty shall be to repair or replace (F.O.B. Seller's plant, Beaverton, Oregon, USA) any goods that are found to be non-conforming or defective as specified by Buyer within 30 days of discovery of any defect. Buyer shall bear all installation and transportation expenses, and all other incidental expenses and damages.

Limitation of Liability. *In no event shall Seller be liable for any type of special consequential, incidental, or penal damages, whether such damages arise from, or are a result of, breach of contract, warranty, tort (including negligence), strict liability, or otherwise.* All references to damages herein shall include, but not be limited to: loss of profit or revenue; loss of use of the goods or associated equipment; costs of substitute goods, equipment, or facilities; downtime costs; or claims for damages. Seller shall not be liable for any loss, claim, expense, or damage caused by, contributed to, or arising out of the acts or omissions of Buyer, whether negligent or otherwise.

No Other Warranties. Seller makes no other warranties, express or implied, including without limitation the implied warranties of merchantability and fitness for a particular purpose, regarding Seller's Products or Documentation. Seller does not warrant, guarantee, or make any representations regarding the use or the results of the use of the Products or Documentation or their correctness, accuracy, reliability, currentness, or otherwise. All risk related to the results and performance of the Products and Documentation is assumed by Buyer. The exclusion of implied warranties is not permitted by some jurisdictions. The above exclusion may not apply to Buyer.

Disclaimer. Seller's Products and Documentation, including this document, are subject to change without notice. Documentation does not represent a commitment from Seller.

Firmware Guide for Camera Link Products

Firmware Guide for Camera Link Products

Overview

This guide describes the firmware for EDT Camera Link products – the C-Link (Camera Link) series and the FOX (fiberoptic) series – including PCI, PCI Express, CompactPCI, and PMC framegrabbers. The firmware described in this guide is related to the user interface (UI) FPGA, which communicates with the camera.

Your EDT installation package includes specific firmware files for each EDT product. For a list of these files, and for details on querying and loading the FPGA using the `pciload` utility, consult the documentation for EDT framegrabbers (see Related Resources below).

Purpose

The purpose of this guide is to help users understand EDT's digital video products and their underlying logic, as accessed by the EDT API and camera configuration tools and files (see Related Resources on page 2).

If you choose to access the registers directly or write your own drivers, EDT cannot provide support. Therefore, we recommend using only the EDT API and camera configuration resources for programming EDT digital video products.

Related Resources

The resources below may be helpful or necessary for your applications.

- To find complete details on any EDT product, go to www.edt.com and find the appropriate product page. That page will provide links to the product's datasheet specifications and user's guide.
- To find EDT information that is not related to a specific EDT product (such as installation packages, or cable pinouts that apply to multiple products), go to www.edt.com and look in Product Documentation.

EDT Documentation	Detail	Web link
• Application programming interface (API)	HTML and PDF versions	www.edt.com/manuals.html
• Installation packages (Windows, Linux, etc.)	Software / firmware	www.edt.com/software.html
• EDT main boards (PCI SS, PCI GS, PCIe8 LX)	User's guide	www.edt.com/manuals/PCD/main_boards.pdf
• EDT framegrabbers / digital video products	User's guide	www.edt.com/manuals/PDV/pcidv.pdf
	Datasheet for each product	www.edt.com (see product page)
• Cabling and pinouts	Addendum	" (see Product Documentation)
• Camera Configuration Guide	Addendum	www.edt.com/manuals/PDV/camconfig.pdf

Standard / Specification	For	From	Web link
• PCI / PCIe	PCI / PCIe bus	PCI Special Interest Group (PCI SIG)	www.pcisig.com
• Camera Link	Camera Link	Machine Vision Online (MVO)	www.machinevisiononline.org

Pinouts

Each EDT framegrabber has two MDR-26 Camera Link connectors:

- The primary connector is closest to the bus connector, and is labeled with the lesser value (“0” on PCI Express boards, “1” on PCI boards). It is linked to logical channel 0.
- The secondary connector is farthest from the bus connector, and is labeled with the greater value (“1” on PCI Express boards, “2” on PCI boards). It is linked to logical channel 1.

The primary connector is used for one base-mode camera. The secondary connector can be used for a second base-mode camera, or for the secondary connector of a medium-or full-mode camera.

Below are the pin assignments for base-, medium-, and full-mode systems.

Pin on camera end	Pin on framegrabber end	Camera Link signal, base mode (primary connector)	Camera Link signal, medium mode (secondary connector)	Camera Link signal, full mode (secondary connector)
1	1	inner shield	inner shield	inner shield
14	14	inner shield	inner shield	inner shield
2	25	X0–	Y0–	Y0–
15	12	X0+	Y0+	Y0+
3	24	X1–	Y1–	Y1–
16	11	X1+	Y1+	Y1+
4	23	X2–	Y2–	Y2–
17	10	X2+	Y2+	Y2+
5	22	Xclk–	Yclk–	Yclk–
18	9	Xclk+	Yclk+	Yclk+
6	21	X3–	Y3–	Y3–
19	8	X3+	Y3+	Y3+
7	20	SerTC+	unused	100 ohms
20	7	SerTC–	unused	terminated
8	19	SerTFG–	unused	Z0–
21	6	SerTFG+	unused	Z0+
9	18	CC1–	unused	Z1–
22	5	CC1+	unused	Z1+
10	17	CC2+	unused	Z2–
23	4	CC2–	unused	Z2+
11	16	CC3–	unused	Zclk–
24	3	CC3+	unused	Zclk+
12	15	CC4+	unused	Z3–
25	2	CC4–	unused	Z3+
13	13	inner shield	inner shield	inner shield
26	26	inner shield	inner shield	inner shield

About the Registers

Your EDT installation package provides firmware files for accessing the various registers described below.

User Interface (UI) FPGA Registers

The EDT driver on the host computer uses the registers described in this document and implemented in the user interface (UI) FPGA, sometimes called the remote FPGA, to control the camera.

As camera data passes through the FPGA, the registers affect the data pipeline as follows:

- If region of interest is enabled — that is, if bit 3, ROIDIS, in 0x29 Camera Link Control is false — then the region-of-interest counters apply.
- Following the formats described in the Camera Link specification (see Related Resources on page 2), arrange data from the camera into taps as determined by 0x28 Camera Link Data Path.
- Unless bit 0, EXT_DEPTH, in 0x06 Data Path is set, each tap is truncated to the eight most significant bits, as if the camera were eight bits per tap. Otherwise, the correct number of taps, and bits per tap, can be set for your camera as follows:
  - If bit 0, RGB, is set in 0x29 Camera Link Control, then this overrides any setting in 0x28 Camera Link Data Path. Data is assumed to come from an RGB color camera with three taps (one each for red, green, and blue) of eight bits each.
  - Otherwise, the number of taps and bits per tap can be set in 0x28 Camera Link Data Path.

In any case, the image data from all taps is packed into 32-bit data words as described in 0x28 Camera Link Data Path on page 15.

Bits 0 and 3, BSWAP and SSWAP, in 0x0F Utility also affect the ordering of the data.

Camera Interface Registers

The access to the camera interface registers depends on how you are using the primary connector (the one closer to the bus connector) and the secondary connector (the one farther from the bus connector):

- Primary addresses (0x00 through 0x35) are for all cameras on the primary connector, and medium- and full-mode cameras on the secondary connector.
- Secondary addresses (starting at 0x40) are for base-mode cameras on the secondary connector.

NOTE Each secondary address is the same as its corresponding primary address, but offset by 0x40. When setting and getting registers on the secondary connector with such API calls as `edt_reg_read` and `edt_reg_write`, the driver applies the offset automatically based on the handle returned from `pdv_open_channel`. Therefore, use the primary address in nearly all cases when using these calls.

Camera Interface Registers: Primary Addresses

These primary addresses are for all cameras on the framegrabber's primary connector, and for medium- and full-mode cameras on the framegrabber's secondary connector.

0x00 Command

Access / Notes: 8-bit write-only / PCD_CMD (secondary address = 0x40)

Bits written to this register do not retain state after writing; there is no need to clear them after setting them.

When read, this register is 0x00 Firmware ID, which follows this one.

Bit	Access	Name	Description
7–5		[no name]	Not used.
4		CLRFVINT	Set to clear the frame-valid interrupt, found in the 0x0B Serial Data Status.
3		CLEAR_CONT	Set to clear bit 4, CONTINUOUS, in 0x06 Data Path the next time bit 7, AQUIRE_IP, in 0x01 Status is set. If the latter bit is set already when this bit is toggled, the CONTINUOUS bit is cleared immediately.
2		AQ_CLR	When set, resets bit 5, AQUIRE_INT, in 0x0B Serial Data Status.
1		ENABLE_GRAB	Set to cause the framegrabber to enter the armed state. When armed, the framegrabber starts acquiring data with the next rising edge of the frame-valid signal. The framegrabber exits the armed state when data acquisition starts, unless the CONTINUOUS bit in 0x06 Data Path is set, in which case the framegrabber remains armed for subsequent frames.
0		RESET_INTFC	Set to reset the PCI DV camera interface circuit. This clears the ACQUIRE and FVAL interrupts, stops current DMA, if any, and returns the board to an idle state.

0x00 Firmware ID

Access / Notes: 8-bit read-only / PDV_REV (secondary address = 0x40)

Bit	Access	Name	Description
7–4		[no name]	Not used.
3–0		REV	The FPGA configuration file revision level.

0x01 Status

Access / Notes: 8-bit read-only / PDV_STAT (secondary address = 0x41)

The executable `watchstat`, included in the EDT installation package, reads and displays this register symbolically.

Bit	Access	Name	Description
7		AQUIRE_IP	When set, the camera interface has detected a valid beginning of frame and is acquiring data.
6		GRAB_ARMED	When set, the grab command has been issued, any specified hardware trigger has been detected, and the camera interface is waiting for a valid beginning of frame.
5		WIRE_TRIG	Status of incoming trigger on serial-to-framegrabber (SERTFG2) UART signal of the secondary connector. If the signal on the secondary connector is not used for something else, this enables the use of the UART signal pair on the secondary connector as a trigger.
4		PHOTO_TRIG	Status of incoming trigger on optocoupler.
3		TRIGGER_ARMED	When set, the grabcommand has been issued and the board is ready for a hardware trigger. This bit is cleared when the above bit 7, AQUIRE_IP, is set, unless bit 2 (the most significant of the three HWTRIG[2–0] bits) also is set in 0x10 Utility 2. See Table 3.
2		EXPOSURE	When set, the camera expose line is asserted.
1		FRAME_VALID	When set, the camera is transmitting a frame of data. This does not necessarily mean that the framegrabber is acquiring data, which also depends on whether the framegrabber was armed at the start of the frame.
0		OVERRUN	When set, indicates that data was lost during a frame transfer because the host was not ready to receive at the rate at which the camera was transmitting. Therefore, the data has become corrupted.

0x02 Configuration

Access / Notes: 8-bit write-only / PDV_CFG (secondary address = 0x42)

Bit	Access	Name	Description
7		INT_ENAQ	Set to enable the acquisition interrupt, which occurs at the rising edge of bit 7, AQUIRE_IN, in 0x01 Status. Clear the interrupt using bit 2, AQ_CLR, in 0x00 Command.
6–4		[no name]	Not used.
3		FIFO_RESET	Toggle this bit to reset the framegrabber input FIFO.
2		INV_SHUTTER	Set to invert the polarity of the shutter signal. When clear, the selected CC line to the camera is positive to trigger the shutter. The shutter signal is assigned to bits 7–4, EN_SHUTTER[4-1], in 0x07 Mode Control.
1–0		[no name]	Not used; always 0.

0x03 Shutter

Access / Notes: 8-bit write-only / PDV_SHUTTER (secondary address = 0x43)

Many cameras determine the exposure time by a serial UART command; in such cases, the camera uses only the leading edge of the shutter signal, not the trailing edge.

Bit	Access	Name	Description
7–0		SHUTTER[7–0]	Specifies the exposure time minus one, in increments of 1 millisecond, 10 ms, or 100 ms — the units are specified by bits 7–6, DECADE[1-0], in 0x06 Data Path. If units are milliseconds, write a value of 2 for a 3 ms exposure; if units are 10 ms, write a value of 2 for a 30 ms exposure; and so on.

0x03 Shutter Time Left

Access / Notes: 8-bit read-only / PDV_SHUTTER_LEFT (secondary address = 0x44)

Bit	Access	Name	Description
7–0		SHUTTER_LEFT [7–0]	Reads the amount of time left before the current exposure terminates. The units are specified by bits 7–6, DECADE[1-0], in 0x06 Data Path.

0x05 Utility 3

Access / Notes: 8-bit read-write / PDV_UTIL3 (secondary address = 0x45)

To avoid undefined operation, do not set both bit 6 and bit 7. For details on how these two bits work together to define frame rate counter behavior, see Table 1 on page 8.

Bit	Access	Name	
7		FRENA	Use the frame rate counter (bits 23–0, FRATE, in 0x14–16 Frame Rate Bytes 0–2) to generate a constant frame rate trigger to the camera.
6		FVADJ	Use the frame rate counter (bits 23–0, FRATE, in 0x14–16 Frame Rate Bytes 0–2) to adjust the length of frame valid for holding off next frame.
5–4		[no name]	Not used.
3		FVINTPOL	When clear, the frame-valid interrupt occurs on the falling edge of the frame-valid signal from the camera. When set, the frame-valid interrupt occurs instead on the rising edge of the signal.
2		EXPINT	Select the EXPOSE signal to camera as the source of the frame-valid interrupt, instead of the frame-valid signal from the camera.
1		[no name]	Not used.
0		PTRIGINV	When set and then triggered from an external device — either optical or SERTFG2 trigger — the incoming trigger polarity is inverted so that negative is true.

Table 1. Frame rate counter behavior

Bits 7–6, FRENA and FVADJ, in 0x05 Utility 3 interact as below. To avoid undefined behavior, do not set both.

0x05 bit 7	0x05 bit 6	RESULT
0	0	Frame rate counter not used. Ordinarily, camera is triggered only after the end of the frame-valid signal for the previous frame.
0	1	Use the frame rate counter (0x14–16 Frame Rate Bytes 0–2) to adjust the duration of the frame-valid signal. Useful for cameras that need an additional delay after frame-valid goes false before triggering the next frame: in such cases, set the frame rate counter for a time period longer than that of frame-valid from the camera. For cameras able to accept a new trigegr signal while the previous frame-valid signal is still true, set the counter for a time period shorter than the frame-valid signal.
1	0	Use the frame rate counter to specify a constant frame rate (in microseconds).
1	1	Undefined.

0x06 Data Path

Access / Notes: 8-bit read-write / PDV_DATA_PATH (secondary address = 0x47)

Bit	Access	Name	Description
7–6		DECADE[1–0]	Specifies the units for the shutter counter: **DECADE 1 DECADE 0 Units** 0 0 1 millisecond 0 1 10 milliseconds 1 0 100 milliseconds 1 1 reserved
5		[no name]	Not used.
4		CONTINUOUS	Set if the framegrabber is to acquire successive frames of data. To start acquisition, bit 1, ENABLE_GRAB, in 0x00 Command must be set. After this bit is cleared, acquisition continues until the end of the current frame. Clear this bit in either of two ways: write a 0 to clear it immediately, or toggle bit 3, CLEAR_CONT, of 0x00 Command to clear this bit after the next DMA transfer completes.
3–1		[no name]	Not used.
0		EXT_DEPTH	Set to send full camera bit depth to the host for each pixel from the camera. Clear to send only the eight most significant bits of each pixel. This bit is set automatically if the `extdepth` camera configuration directive is greater than eight in the camera cofiguration file

0x07 Mode Control

Access / Notes: 8-bit read-write / PDV_MODE_CNTL (secondary address = 0x47)

Bit	Access	Name	Description
7–4		EN_SHUTTER[4–1]	Set which camera control signal is driven by the internal EXPOSE signal from the shutter timer. If all bits are 0, no EXPOSE signal is sent to the camera. If one of these bits is asserted while the framegrabber is in continuous mode, the shutter timer asserts EXPOSE to the camera to trigger each frame. Ordinarily, just one of these bits is true (for most cameras, the least significant bit). However, the following combinations select nonstandard behavior: 1010 Drives CC1 with the trigger signal from the optocoupler. 1011 Drives CC2 from the optocoupler; CC1, CC3, CC4 all forced low. 110– Drives CC4 with frame-valid from the camera, for those frames sent to the host. (The – notation for the least significant bit signifies “don’t care”.)
3–0		CC[4–1]	Sets the state of the camera control outputs, unless the output is enabled as a shutter using bits 7–4, EN_SHUTTER[4–1], described above.

0x0A Serial Data

Access / Notes: 8-bit read-write / PDV_SERIAL_DATA (secondary address = 0x4A)

Together, 0x0A, 0x0B, and 0x0C implement an asynchronous UART in the FPGA to communicate with the camera. Serial control lines are eight data bits, one stop bit, no parity.

Bit	Access	Name	Description
7–0		SERIAL_DATA[7–0]	If bit 1, TRANSMIT_READY, is set in 0x0B Serial Data Status, this register (0x0A) is ready to have data written to it. The data then is output on the signal SERTC (the serial line to the camera). When bit 0, RECEIVE_RDY, in 0x0B Serial Data Status is set, the data read from this register will reflect the last character received.

0x0B Serial Data Status

Access / Notes: 8-bit read-only / PDV_SERIAL_DATA_STAT (secondary address = 0x4B)

Together, 0x0A, 0x0B, and 0x0C implement an asynchronous UART in the FPGA to communicate with the camera. Serial control lines are eight data bits, one stop bit, no parity.

See Table 2 on page 10 for the six sources of a frame-valid interrupt signal.

Bit	Access	Name	Description
7		INTFC_INT	Set when: (TRANSMIT_RDY AND EN_TX_INT) OR (RECEIVE_RDY AND EN_RX_INT) OR AQUIRE_INT OR FVINTSTAT The expression that set this bit then is ANDed with bit 4, EN_GLOB_INT, in 0x0C Serial Data Control. The result is passed to the PCI FPGA. An interrupt then is asserted over the PCI bus to the host computer if these two additional "enable interrupt" bits are set in the 0xC4 PCI Interrupt and UI FPGA Configuration register: bit 15 (EDT_PCI_EN_INTR) and bit 14 (EDT_RMT_EN_INTR) For documentation of the 0xC4 PCI Interrupt and UI FPGA Configuration register, consult the user's guide for EDT main boards (see Related Resources on page 2).
6		FVINT	Set when the frame-valid interrupt is pending (see Table 2 for possible sources). Cleared by bit 4, CLRFVINT, in 0x00 Command.
5		AQUIRE_INT	Set when an acquisition interrupt is enabled through bit 7, INT_ENAQ, of 0x02 Configuration, and a rising edge of bit 7, AQUIRE_IP, in 0x01 Status has been detected. Cleared by bit 2, AQ_CLR, in 0x00 Command.
4		FVINTSTAT	Set when both bit 6, FVINT, in this register and bit 3, ENFVINT, in 0x10 Utility 2 are true.
3–2		[no name]	Not used.
1		TRANSMIT_RDY	Set when the serial data transmitter is enabled and ready for the next character. Clears automatically when character transmission is complete.
0		RECEIVE_RDY	Set when the serial data receiver is enabled and a character isavailable for reading. Cleared by bit 5, CL_RECEIVE_RDY, in 0x0C Serial Data Control.

Table 2. Sources of frame-valid interrupt signal

When the source of a frame-valid interrupt signal occurs, then bit 6, FVINT, in 0x0B Serial Data Status is set.

The source can be any one of six possible sources, depending on interactions among bits 2 and 3, FVINTPOL and EXPINT, in 0x05 Utility 3 and bit 4, PTRIGINT, in 0x10 Utility 2. If bit 3, ENFVINT, in that register also is set (to enable frame-valid interrupt), then bits 4 and 7, FVINTSTAT and INTFC_INT, in 0x0B Serial Data Status are set. The interrupt then is sent under the circumstances described there for bit 7.

0x10 bit 4	0x05 bit 3	0x05 bit 2	RESULT
0	0	0	Frame-valid interrupt on falling edge of frame-valid signal.
0	0	1	Frame-valid interrupt on rising edge of frame-valid signal.
0	1	0	Frame-valid interrupt on falling edge of expose signal (typically, from the shutter timer).
0	1	1	Frame-valid interrupt on rising edge of expose signal (typically, from the shutter timer).
1	–	0	Frame-valid interrupt on falling edge of signal from optocoupler.
1	–	1	Frame-valid interrupt on rising edge of signal from optocoupler.

The notation "–" means that the value of the bit does not affect the result.

0x0C Serial Data Control

Access / Notes: 8-bit read-write / PDV_SERIAL_DATA_CNTL (secondary address = 0x4C)

Together, 0x0A, 0x0B, and 0x0C implement an asynchronous UART in the FPGA to communicate with the camera. Serial control lines are eight data bits, one stop bit, no parity.

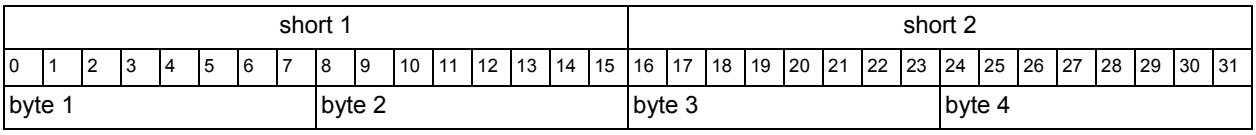
Bit	Access	Name	Description
7–6		BAUD[1–0]	Sets the serial port baud rate for serial data: **BAUD 1 BAUD 0 BAUD RATE** 0 0 9600 0 1 19200 1 0 38400 1 1 115200 If these choices are insufficient, it is possible to override this value and set an arbitrary baud rate using 0x24 Baud Rate.
5		CL_RECEIVE_RDY	Set to clear bit 0, RECEIVE_RDY, in 0x0B Serial Data Status.
4		EN_GLOB_INT	Enables all interrupts.
3		EN_TX_INT	Enables the TRANSMIT_RDY interrupt.
2		EN_RX_INT	Enables the RECEIVE_RDY interrupt.
1		EN_TX	Enables the serial data transmitter.
0		EN_RX	Enables the serial data receiver.

0x0F Utility

Access / Notes: 8-bit read-write / PDV_UTILITY (secondary address = 0x4F)

Bit	Access	Name	Description
7–6		[no name]	Not used.
5		HWTRIGEXP	When set, the EXPOSE line to the camera comes from the user's trigger input, either through the optocoupler or from SERTFG2, depending on bits 2–0, HWTRIG[2–0], in 0x10 Utility 2. Bits 4–1, CC[4–1], in 0x07 Mode Control determine which of the four camera control lines will carry the EXPOSE signal to the camera.
4		[no name]	Not used.
3		SSWAP	Swaps the order of the two 16-bit short words in one 32-bit data word, so that *short 2* is transferred before *short 1* (equivalent to a byte order of 3,4,1,2). Does not change the order of the bits within each short. Figure 1 shows the structure of a 32-bit data word.
2–1		[no name]	Not used.
0		BSWAP	Swaps the order of bytes 1 and 2, and also bytes 3 and 4, in a 32-bit data word, so that the bytes are transferred in the order 2, 1, 4, 3. Does not change the order of the bits within each byte. Figure 1 shows the structure of a 32-bit data word.

Figure 1. Structure of 32-bit data word



Hardware Triggering

By default, each time the application sets bit 1, ENABLE_GRAB, in 0x00 Command, the camera interface grabs a single frame from the camera. However, if bit 4, CONTINUOUS, in 0x06 Data Path also is set, then the camera interface instead grabs successive frames continuously, as quickly as possible.

Hardware triggering provides additional flexibility. After bit 1, ENABLE_GRAB, in 0x00 Command is set, acquisition is delayed until a hardware trigger is received. What happens next depends on how the interface is configured: it can grab a single frame, a single frame for each hardware trigger, or grab frames continuously after a single hardware trigger.

The optocoupler on the EDT framegrabber is ordinarily the source of the hardware trigger. An easy way to connect to the framegrabber's optocoupler pins is to use the PCI (or PCIe) trigger input backpanel (EDT part #017-02792), which uses a standard female DB9 connector. Drive the signal into pins 2 and 3 of the DB9 connector at 5 V, 10 mA; either polarity is acceptable.

The state of the SERTFG2 line can be read in bit 5, WIRETRIG, of 0x01 Status.

To use the SERTFG2 signal as the hardware trigger source, see Table 3, which presents the possible methods of hardware triggering and the bit combinations necessary to use them.

Table 3. Hardware triggering behavior

Bit 4, CONTINUOUS, is in 0x06 Data Path; bits 2–0, HWTRIG[2–0], are in 0x10 Utility 2. Bit combinations not shown are undefined.

0x06 bit 4	0x10 bit 2	0x10 bit 1	0x10 bit 0	RESULT
0	0	0	0	Acquire the next single frame.
0	0	0	1	Wait for a trigger signal from the application, then acquire a single frame.
0	0	1	0	Wait for a trigger signal from the SERTFG2 signal, then acquire a single frame.
1	0	0	0	Acquire frames continuously.
1	0	0	1	Acquire a frame for each optocoupler trigger.
1	0	1	0	Acquire a frame for each SERTFG2 trigger.
1	1	0	1	Wait for a trigger signal from the optocoupler, then acquire frames continuously.
1	1	1	0	Wait for a trigger signal from the SERTFG2 signal, then acquire frames continuously.

0x10 Utility 2

Access / Notes: 8-bit read-write / PDV_UTIL2 (secondary address = 0x50)

Bit	Access	Name	Description
7		PTRIGSEL	Only for boards including, and newer than, the PCIe8 DV C-Link. 0 (default) = An input trigger on the TRIG0 pin triggers the EXPOSE line. 1 = An input trigger on the TRIG1 pin triggers the EXPOSE line.
6		[no name]	Not used.
5		PULNIX	Set for some Pulnix cameras — see EDT's default camera configuration file for your model, or the Pulnix camera documentation. Allows EXPOSE to the camera to be asserted even when the incoming frame-valid line is true; waits until the end of EXPOSE before bit 6, GRAB_ARMED, in 0x01 Status goes true.
4		PTRIGINT	Set to select the optocoupler as the source of the frame-valid interrupt.
3		ENFVINT	Set to enable the frame-valid interrupt, which ordinarily occurs on the falling edge of frame valid. Clear with bit 4, CLRFVINT, in 0x00 Command.
2–0		HWTRIG[2–0]	Selects the method of hardware triggering, as shown in Table 3 on page 12.

0x14–16 Frame Rate Bytes 0–2

Access / Notes: 8-bit (24-bit in all) read-write / PDV_FRAME_PERIOD0, PDV_FRAME_PERIOD1, PDV_FRAME_PERIOD2 (secondary address = 0x54–56)

Bit	Access	Name	Description
23–0		FRATE[23-0]	A 24-bit preloaded value for the frame rate counter. The counter counts down using microsecond units. For a constant frame rate of *n* microseconds, preload these registers with *n*–2. For example, for a constant frame rate of one hundred frames per second (10,000 μsec per frame), preload a value of 9998, or 0x00270E. These bits are also used to adjust the frame-valid signal duration so that the framegrabber can trigger the camera for the next frame either before or after the previous frame has finished transferring. Bits 7–6, FRENA and FVADJ, in 0x05 Utility 3 will determine how the frame rate counter is used. For details, see Table 1 on page 8.

Region of Interest

Your EDT framegrabber allows you to define a rectangular region of interest. You can then crop your image horizontally, vertically, or both to eliminate superfluous pixels.

Unless disabled by bit 3, ROIDIS, in 0x29 Camera Link Control, the region-of-interest logic is available. To acquire the full image, the region of interest can be set to the full size. Alternatively, the region of interest can be set to be larger than the frame size, to stretch the line-valid and frame-valid signals past the point at which they typically would end.

The region-of-interest registers are 16-bit write-only registers. If region of interest has not been disabled, together these registers define the size of the region of interest.

The examples below assume an image 1024 pixels wide and high with a 10-pixel border on all four sides that are to be cropped; thus, the region of interest is 1004 by 1004.

0x18 Horizontal Skip

Access / Notes: 16-bit write-only / PDV_HSKIP (secondary address = 0x58)

Bit	Access	Name	Description
15–0		HSKIP[15–0]	Write a 16-bit integer to specify the number of pixels to skip at the start of each line. For example, to skip the first ten pixels of each line, load with 0x000A.

0x1A Horizontal Active

Access / Notes: 16-bit write-only / PDV_HACTV (secondary address = 0x5A)

Bit	Access	Name	Description
15–0		HACT[15–0]	Write a 16-bit integer to specify the number of pixels minus one (*pixels* –1) to transfer on each line, after the HSKIP pixels have been skipped. For example, to acquire 1004 pixels on each line, load with 0x03EB.

0x1C Vertical Skip

Access / Notes: 16-bit write-only / PDV_VSKIP (secondary address = 0x5C)

Bit	Access	Name	Description
15–0		VSKIP[15–0]	Write a 16-bit integer to specify the number of lines to skip at the start of each frame. For example, to skip the first ten lines of each frame, load with 0x000A.

0x1E Vertical Active

Access / Notes: 16-bit write-only / PDV_VACTV (secondary address = 0x5E)

Bit	Access	Name	Description
15–0		VACT[15–0]	Write a 16-bit integer to specify the number of lines minus one(*lines* –1) to transfer in each frame, after the VSKIP lines have been skipped. For example, to acquire 1004 lines in each frame, load with 0x03EB.

0x24 Baud Rate

Access / Notes: 8-bit read-write / PDV_BRATE (secondary address = 0x64)

Bit	Access	Name	Description

7–0		BRATE[7–0]	Sets the UART baud rate to the value specified. A value of zero specifies that the UART baud rate is set by bits 7–6, BAUD[1–0], in Table 2 on page 10.
			
			Given a required baud rate of *baud_rate*:
			
			`BRATE[7-0] = (20 MHz / (`*baud_rate*` * 16))-2`
			
			Round to the nearest integer; however, make sure that such rounding introduces an error less than 5%. (This is a problem only for high baud rates.) If the error is greater than 5%, the camera serial control may not operate reliably.
			
			For example, to set a baud rate of 9600...
			
			`20000000/(9600*16)-2 = 128.2`
			
			...so load this register with the value 0x80.

0x28 Camera Link Data Path

Access / Notes: 8-bit read-write / PDV_CL_DATA_PATH (secondary address = 0x68)

Describes the camera in use (numbers of taps and bits per tap) so that the data path can be set up accordingly. Loads automatically with the setting of the `CL_DATA_PATH_NORM` directive in the camera configuration file, if one is present.

For supported values, see Table 4 on page 16; all other values give undefined results.

Bit	Access	Name	Description
7–4		[no name]	The number of data taps, minus one.
3–0		BITS[3–0]	The number of bits per pixel, minus one.

NOTE If bit 0, RGB, in 0x29 Camera Link Control is set, the setting in this register (0x28) is ignored.

Table 4. Data packing

For efficient DMA transfer, image data from all taps is packed into 32-bit (PCI bus) or 64-bit (PCI Express bus) DMA transfer words as shown below.

NUMBER OF TAPS	BITS PER TAP	RESULT
1	8	One byte per Camera Link clock cycle until enough bytes are accumulated to fill DMA transfer word.
2	8	Two bytes per Camera Link clock cycle until enough bytes are accumulated to fill DMA transfer word.
1	10, 12, 14, 16	Two bytes per Camera Link clock cycle in least significant bits of short (16-bit) DMA transfer words, with zeroes as padding in most significant bits as needed.
2	10, 12, 14, 16	Four bytes per Camera Link clock cycle in least significant bits of short (16-bit) data words; see Figure 2.
3	8	Three bytes per Camera Link clock cycle, densely packed; see Figure 3. **NOTE:** Requires setting bit 0 in 0x29 Camera Link Control instead of using 0x28 Camera Link Data Path.
4 (medium mode)	8	Four bytes per Camera Link clock cycle, with no padding. Happens automatically as a consequence of loading the framegrabber with medium-mode firmware.

Figure 2. 2-tap 12-bit camera – structure of a 32-bit data word (X is data, 0 is padding)

second tap																first tap															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X

Figure 3. 3-tap 8-bit (RGB) camera – structure of three consecutive 32-bit data words

second pixel								first pixel																							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	B	B	B	B	B	B	B	B	G	G	G	G	G	G	G	G	R	R	R	R	R	R	R	R

third pixel																second pixel															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G	G	G	G	G	G	G	G	R	R	R	R	R	R	R	R	B	B	B	B	B	B	B	B	G	G	G	G	G	G	G	G

fourth pixel																								third pixel							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	B	B	B	B	B	B	B	G	G	G	G	G	G	G	G	R	R	R	R	R	R	R	R	B	B	B	B	B	B	B	B

0x29 Camera Link Control

Access / Notes: 8-bit read-write / PDV_CL_CFG (secondary address = 0x69)

Loads automatically with the setting of the `CL_CFG_NORM` directive in the camera configuration file, if one is present.

Bit	Access	Name	Description
7		ENROIPAD	Set to enable region-of-interest padding. As of revision 36 or later of `pdvcamlk` firmware, if the width or height of incoming data comes up short due to data loss,the region-of-interest logic no longer pads with extra bytes. Setting this bit will reenable the earlier functionality. To enable region-of-interest for width only (useful for linescan cameras), set both this bit and bit 3, ROIDIS, in this register. **NOTE:** Setting this bit (or using older firmware) can mask timeouts because lost data is padded before the image reaches the device driver, resulting in a persistent out-of-synch condition. The application then will not be notified when it needs to perform timeout recovery.
6		RGBSWAP	Set to swap red (R) and blue (B) bytes in RGB triplets, so that they become BGR.
5		DVINV	Set to invert the data-valid signal, for the few cameras that require this.
4		FVALGEN	For linescan cameras; enables internal generation of frame valid after VACTV lines. Set bit 2, LINESCAN, when using this feature.
3		ROIDIS	Set to disable the region-of-interest counters, thus always acquiring the entire image. (These counters are set in0x18 Horizontal Skip, 0x1C Vertical Skip, 0x1C Vertical Skip, and 0x1E Vertical Active.) To enable region-of-interest for width only (useful for linescan cameras), set both this bit and bit 7, ENROIPAD, in this register.
2		LINESCAN	Set to replace the frame-valid signal from the camera with a copy of the line-valid signal.
1		IGNDVAL	Set if the camera does not implement the data-valid output signal.
0		RGB	Set if the camera is 24-bit color: 8 bits each per red, green, and blue taps. If this bit is set, it overrides any setting in 0x28 Camera Link Data Path.

0x2A, 2B Lines Per Frame

Access / Notes: 16-bit read-only / PDV_CL_LINESPERFRAME (secondary address = 6A, 6B)

0x2A = PDV_CL_LINESPERFRAME[7–0]
0x2B = PDV_CL_LINESPERFRAME[15–8]

Bit	Access	Name	Description
15–0		LINESPERFRAME	Reports the number of lines per frame; updated after each frame.

0x2C, 2D Pixels Per Line

Access / Notes: 16-bit read-only / PDV_CL_PIXELSPERLINE (secondary address = 6C, 6D)

0x2C = PDV_CL_PIXELSPERLINE[7–0]
0x2D = PDV_CL_PIXELSPERLINE[15–8]

Bit	Access	Name	Description
15–0		PIXELSPERLINE	Reports the number of pixels per line; updated after each line.

0x30 LED

Access / Notes: 8-bit read-write / PDV_CL_LED (no secondary address)

PCI Express boards (`pedvcamlk`) only. For debugging. The LED, in the center of the top edge of the board, is not visible when the board is enclosed in the host case.

Bit	Access	Name	Description
7–3		[no name]	Not used.
2		TOGGLE	If bits 0–1, SELECT, are set: Set this bit to turn on LED; clear this bit to turn off LED.
1–0		SELECT	Set the state of the LED:

BIT 0	BIT 1	RESULT
0	0	Slow blink.
0	1	Blinks when frame valid is high.
1	0	Blinks when line valid is high.
1	1	Lit if bit 2 is set; dark if bit 2 is clear.

0x35 Camera Link Control 2

Access / Notes: 8-bit read-write / PDV_CL_CFG2 (secondary address = 0x75)

Loads automatically with the setting of the `CL_CFG2_NORM` directive in the camera configuration file, if one is present.

For details on triggering, consult the user's guide for EDT framegrabbers (see Related Resources on page 2).

This register is used differently for different products, as indicated below.

PCI DV C-Link:

Bit	Access	Name	Description
7–2		[no name]	Not connected.
1		EXP_SEL	0 (default) = For each connector, EXPOSE is generated via the shutter timer on that connector's corresponding camera module: – for the primary connector, EXPOSE is generated via camera module 0 – for the secondary connector, EXPOSE is generated via camera module 1 1 = For both connectors, EXPOSE is generated via the shutter timer on camera module 0
0		SEPTRIG	0 (default) = An input trigger on the TRIG0 pin triggers both outgoing EXPOSE lines, one for each connector. 1 = An input trigger on the TRIG0 pin triggers the EXPOSE line on the primary connector, and an input trigger on the TRIG1 pin triggers the EXPOSE line on the secondary connector.

PCIe4 DV C-Link:

Bit	Access	Name	Description
7–1		[no name]	Not connected.
0		PTRIGSEL	Used in conjunction with bit 0 in 0x10 Utility 2 (see Table 3 on page 12). 0 (default) = An input trigger on the TRIG0 pin triggers both outgoing EXPOSE lines, one for each connector. 1 = An input trigger on the TRIG0 pin triggers the EXPOSE line on the primary connector, and an input trigger on the TRIG1 pin triggers the EXPOSE line on the secondary connector.

PCIe8 DV C-Link FPGA configuration file – rev. 10 and later:

Bit	Access	Name	Description
7		[no name]	Not connected.
6		[no name]	Not connected.
5		PE8_FRMTAG2	When set, replaces the first two bytes of the frame with frame counter.
4		PE8_FRMTAG	When set, replaces the first two bytes of the frame with FF00.
3		PCLVFREE	When set, puts pixels per line register in freerunmode.
2		OPTO_FRMTRIG	Typically used with linescan cameras. 0 (default) = sets TRIG0 pin as frame trigger when bit 7, PTRIGSEL, in 0x10 Utility 2 is set. **Note:** In the above case, setting bit 0, PTRIGINV, in 0x05 Utility 3 inverts the TRIG0 input. 1 = sets TRIG1 pin as frame trigger when bit 7, PTRIGSEL, in 0x10 Utility 2 is set.
1		[no name]	Not connected.
0		[no name]	Not connected.

Camera Interface Registers: Secondary Addresses

These secondary addresses are only for base-mode cameras on the framegrabber's secondary connector.

When using the API as documented, the channel offset is applied automatically, so any address passed to EDT register manipulation calls (e.g., `edt_reg_write`) should always be the primary address.

0x40 Command

Access / Notes: Same as 0x00.

0x41 Status

Access / Notes: Same as 0x01.

0x42 Configuration

Access / Notes: Same as 0x02.

0x43 Shutter

Access / Notes: Same as 0x03.

0x44 Shutter Time Left

Access / Notes: Same as 0x04.

0x45 Utility 3

Access / Notes: Same as 0x05.

0x46 Data Path

Access / Notes: Same as 0x06.

0x47 Mode Control

Access / Notes: Same as 0x07.

0x40 Firmware ID

Access / Notes: Same as 0x00.

0x4A Serial Data

Access / Notes: Same as 0x0A.

0x4B Serial Data Status

Access / Notes: Same as 0x0B.

0x4C Serial Data Control

Access / Notes: Same as 0x0C.

0x4F Utility

Access / Notes: Same as 0x0F.

0x50 Utility 2

Access / Notes: Same as 0x10.

0x54–56 Frame Rate Bytes 0–2

Access / Notes: Same as 0x14–16.

0x58 Horizontal Skip

Access / Notes: Same as 0x18.

0x5A Horizontal Active

Access / Notes: Same as 0x1A.

0x5C Vertical Skip

Access / Notes: Same as 0x1C.

0x5E Vertical Active

Access / Notes: Same as 0x1E.

0x64 Baud Rate

Access / Notes: Same as 0x24.

0x68 Camera Link Data Path

Access / Notes: Same as 0x28.

0x69 Camera Link Control

Access / Notes: Same as 0x29.

0x6A, 6B Lines Per Frame

Access / Notes: Same as 0x2A, 2B.

0x6C, 6D Pixels Per Line

Access / Notes: Same as 0x2C, 2D.

0x75 Camera Link Control 2

Access / Notes: Same as 0x35.

Revision Log

Below is a history of modifications to this guide.

Date	Rev	By	Pp	Detail
20110402	06	PH	All	• Implemented new formats and minor corrections; added Revision Log.
20090000	00-05	LW	All	• Created new guide and implemented updates.