PCI DV

Addendum A: AIA Generic

For use with:

PCI DV
PCI DVa
PCI DVK
PMC DVK
PCI DV44
PCI RCI System
PCI RCI Module

Revision: B
February 2003

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Contents

Overview

The PCI DV is a single-slot PCI Bus board that implements a high-speed DMA channel between an external digital video camera and a host computer. The device interface side of the board consists of 35 differential driver/receivers connected to a Xilinx RAM-based programmable gate array. These driver/receivers can be assigned as inputs or outputs in groups of four. In the standard configuration, drivers are RS-422 and receivers are EIA-644 (LVDS). Other configurations are available. The Xilinx device can be programmed to implement arbitrary interface protocols by executing a program that downloads a bit pattern from a file to the PCI DV board.

Some versions of the firmware allow you to enable a *region of interest*, a rectangle you can define to crop an image horizontally and vertically, thus eliminating superfluous pixels.

This document describes the PCI DV firmware for a wide range of digital cameras that send 16 data bits or fewer per video clock cycle. Many of these cameras follow the specification for AIA Monochrome Digital Cameras (see References, page 38, for the complete specification reference). To handle variations among cameras, EDT provides special cables, programmable registers, and in some cases special Xilinx firmware configuration files.

For further information about using the PCI DV, contact EDT and ask for the *PCI DV User's Guide* (part number 008-00966).

Throughout this guide, the term "PCI DV" is used generically. Except where noted, it can be assumed that PCI DV refers to all the products in the PCI DV family.

Xilinx Firmware

The logic for the registers described in this addendum is contained in a Xilinx firmware file that is resident in an on-board PROM. Field upgrades to this PROM may occasionally be necessary when upgrading to a new device driver.

The following files, included in the PCI DV software/driver package under the base directory (typically c:\EDT\pdv in MS Windows installations, and /opt/EDTpdv in Unix/Linux installations), are used to check and upgrade the firmware:

pciload	Xilinx download utility, UNIX version
pciload.exe	Xilinx download utility, MS Windows version
flash/4013e/pcidv_3v.bit	PCI DV Xilinx bitfile for 3v sector, 4013e version
flash/4013e/pcidv_5v.bit	PCI DV Xilinx bitfile for 5v sector, 4013e version
flash/4028xla/pcidv_3v.bit	PCI DV Xilinx bitfile for 3v sector, 4028xla version
flash/4028xla/pcidv_5v.bit	PCI DV Xilinx bitfile for 5v sector, 4028xla version
flash/4013xla/pdvk_3v.bit	PCI DVK Xilinx bitfile for 3v sector, 4013xla version
flash/4013xla/pdvk_5v.bit	PCI DVK Xilinx bitfile for 5v sector, 4013xla version
flash/4013xla/pcidv44_3v.bit	PCI DV44 Xilinx bitfile for 3v sector, 4013xla version
flash/4013xla/pcidv44_5v.bit	PCI DV44 Xilinx bitfile for 5v sector, 4013xla version
flash/4013e/pcidv.bit	PCI DV Xilinx bitfile, 4013e version
flash/4013e/pdvk.bit	PCI DVK Xilinx bitfile, 4013e version

Upgrading the interface PROM involves downloading the firmware to the board's PCI Xilinx flash PROM using the pciload program.

To compare the current PCI Xilinx files in the package (from the above file list) with the files currently in the PROM on the PCI DV, run:

```
pciload verify
```

Pciload verify will find the matching file in the flash directoy and perform a comparison, then output the PROM, file IDs, and revision dates. If they differ, upgrade the PROM with the new file as follows:

```
pciload update
```

If you have multiple EDT boards in the system, use the -u flag to specify which unit to verify or upgrade. The first unit is 0. For example, to upgrade the first unit, use -u 0:

```
pciload -u 0 update
```

The board only reloads this from flash when being powered up, so after running pciload, the new bit file will not be in the Xilinx until the system has power cycled. This requires cycling power, not just rebooting.

For a list of all possible options to pciload, run:

```
pciload -h
```

Connector Pinout

The PCI DV uses a high-density 80-pin I/O connector. Many digital cameras use a 68-pin female high-density connector that follows the *AIA Monochrome Digital Camera with Category I Extended Interface* specification. EDT can provide appropriate cables that adapt the PCI DV board to these or other cameras.

The 68-pin male cable connector used with many of these cameras is AMP part number 749621-7, with a shielded backshell (AMP part number 750752-1).

The PCI DVK and PCI RCI use use a high-density 68-pin I/O connector, allowing straight-through connection to those cameras. The PCI DV 44 has a three-row 44-pin connector and is used with cameras from DVC.

The following definitions may prove helpful in understanding the pinout diagrams:

MSB	Most significant bit. MSB[0-15] are the data lines. Of these, MSB15 is the least significant.
AMSB	Most significant bit, A channel (dual channel operation)
BMSB	Most significant bit, B channel (dual channel operation)
SCNTLI	Serial control input to the camera for the RS-422 serial port.
SCNTLO	Serial control output from the camera to the PCIDV.
LINE	Line valid signal. When asserted with Frame Valid, valid pixel data is being transmitted.
FRME	Frame valid signal. Asserted from beginning to end of frame.
MC	Mode control lines. MC[0-2] are Kodak mode control lines 0-2, and AIA mode control lines 1-3.
EXPOSE	Frame reset (to trigger a new frame) / Exposure (length of exposure). This is the Kodak shutter control line, or AIA mode control line 0. A duplicate of this signal may go out as EXPOSEB.

The following pinout diagrams describe the connection from the cable to these cameras. The connection from the PCI DV board to the cable is described in the *PCI DV Family User's Guide* (part number 008-00966), available at www.edt.com.

PCI DV Pin	PCI DV Signal	AIA Signal	PCI DV Pin	PCI DV Signal	AIA Signal
1	Ground	Not used	41	Ground	Not used
2	Ground	Not used	42	Ground	Not used
3	VD4 +	MSB4 +	43	VD0 +	MSB0 +
4	VD4 –	MSB4 –	44	VD0 –	MSB0 –
5	VD5 +	MSB5 +	45	VD1 +	MSB1 +
6	VD5 –	MSB5 –	46	VD1 –	MSB1 –
7	VD6 +	MSB6 +	47	VD2 +	MSB2 +
8	VD6 –	MSB6 –	48	VD2 –	MSB2 –
9	VD7 +	MSB7 +	49	VD3 +	MSB3 +
10	VD7 –	MSB7 –	50	VD3 –	MSB3 –
11	VD12 +	MSB12 +	51	VD8 +	MSB8 +
12	VD12 –	MSB12 –	52	VD8 –	MSB8 –
13	VD13 +	MSB13 +	53	VD9 +	MSB9 +
14	VD13 –	MSB13 –	54	VD9 –	MSB9 –
15	VD14 +	MSB14 +	55	VD10 +	MSB10 +
16	VD14 –	MSB14 –	56	VD10 –	MSB10 –
17	VD15 +	MSB15 +	57	VD11 +	MSB11 +
18	VD15 –	MSB15 –	58	VD11 –	MSB11 –
19	Spare16 +	Not used	59	Spare16 –	Not used
20	+5V	Not used	60	+5V	Not used
21	Spare17 +	Not used	61	Spare17 –	Not used
22	Spare18 +	Not used	62	Spare18 –	Not used
23	Ground	Not used	63	Ground	Not used
24	SCNTLO +	Serial Control Out +	64	PSTRB +	Pixel Strobe +
25	SCNTLO –	Serial Control Out –	65	PSTRB –	Pixel Strobe –
26	ID0 +	Channel ID 0 +	66	LINE +	Line Enable +
27	ID0 –	Channel ID 0 –	67	LINE –	Line Enable –
28	ID1 +	Channel ID 1 +	68	FRME +	Frame Enable +
29	ID1 –	Channel ID 1 –	69	FRME –	Frame Enable –
30	Spare7 +	Not used	70	FLDID +	Field ID +
31	Spare7 –	Not used	71	FLDID –	Field ID –
32	SCNTLI +	Serial Control In +	72	MC0 +	Mode Control 0 +
33	SCNTLI –	Serial Control In –	73	MC0 –	Mode Control 0 –
34	Spare13 +	Not used	74	MC1+	Mode Control 1 +
35	Spare13 –	Not used	75	MC1 –	Mode Control 1 –
36	Spare14 +	Not used	76	MC2 +	Mode Control 2 +
37	Spare14 –	Not used	77	MC2 –	Mode Control 2 –
38	EXPOSEB +	Not used	78	EXPOSE +	FRMRST/EXP +
39	EXPOSEB –	Not used	79	EXPOSE –	FRMRST/EXP –
40	Ground	Ground	80	Ground	Ground

Table 1. PCI DV for Single-channel Grayscale Cameras

Shading denotes out to camera.

PCI DV Pin	PCI DV Signal	AIA Signal	PCI DV Pin	PCI DV Signal	AIA Signal
1	Ground	Not used	41	Ground	Ground
2	Ground	Not used	42	Ground	Not used
3	VDA4 +	AMSB4 +	43	VDA0 +	AMSB +
4	VDA4 –	AMSB4 –	44	VDA0 –	AMSB –
5	VDA5 +	AMSB5 +	45	VDA1 +	AMSB1 +
6	VDA5 –	AMSB5 –	46	VDA1 –	AMSB1 –
7	VDA6 +	AMSB6 +	47	VDA2 +	AMSB2 +
8	VDA6 –	AMSB6 –	48	VDA2 –	AMSB2 –
9	VDA7 +	AMSB7 +	49	VDA3 +	AMSB3 +
10	VDA7 –	AMSB7 –	50	VDA3 –	AMSB3 –
11	VDB4 +	BMSB4 +	51	VDB0 +	BMSB +
12	VDB4 –	BMSB4 –	52	VDB0 –	BMSB –
13	VDB5 +	BMSB5 +	53	VDB1 +	BMSB1 +
14	VDB5 –	BMSB5 –	54	VDB1 –	BMSB1 –
15	VDB6 +	BMSB6 +	55	VDB2 +	BMSB2 +
16	VDB6 –	BMSB6 –	56	VDB2 –	BMSB2 –
17	VDB7 +	BMSB7 +	57	VDB3 +	BMSB3 +
18	VDB7 –	BMSB7 –	58	VDB3 –	BMSB3 –
19	VDA8 +	AMSB8 +	59	VDB8 –	AMSB8 –
20	+5V	+5V	60	+5V	+5V
21	VDA10 +	AMSB10 +	61	VDA10 –	AMSB10 –
22	VDA11 +	AMSB11 +	62	VDA11 –	AMSB11 –
23	Ground	Ground	63	Ground	Ground
24	SCNTLO +	Serial Control Out +	64	PSTRB +	Pixel Strobe +
25	SCNTLO –	Serial Control Out –	65	PSTRB –	Pixel Strobe –
26	VDB10 +	BSMB10 +	66	LINE +	Line Enable +
27	VDB10 –	BSMB10 –	67	LINE –	Line Enable –
28	ID1 +	Bloomflag +	68	FRME +	Frame Enable +
29	ID1 –	Bloomflag –	69	FRME –	Frame Enable –
30	Spare7 +	TRIG +	70	VDB11 +	BMSB11 +
31	Spare7 –	TRIG –	71	VDB11 –	BMSB11 –
32	SCNTLI +	Serial Control In +	72	VDA9 +	AMSB9 +
33	SCNTLI –	Serial Control In –	73	VDA9 –	AMSB9 –
34	Spare13 +	Not used	74	VDB8 +	BMSB8 +
35	Spare13 –	Not used	75	VDB8 –	BMSB8 –
36	Spare14 +	Not used	76	VDB9 +	BMSB9 +
37	Spare14 –	Not used	77	VDB9 –	BMSB9 –
38	EXPOSEB +	FRMRST/EXP +	78	EXPOSE +	Not used
39	EXPOSEB –	FRMRST/EXP –	79	EXPOSE –	Not used
40	Ground	Ground	80	Ground	Ground

Table 2. PCI DV for Dual-channel Grayscale Cameras

Shading denotes out to camera.

PCI DV Pin	PCI DV Signal	AIA Signal	PCI DV Pin	PCI DV Signal	AIA Signal
1	Ground	Not used	41	Ground	Not used
2	Ground	Not used	42	Ground	Not used
3	VDA4 +	RedMSB4 +	43	VDA0 +	RedMSB0 +
4	VDA4 –	RedMSB4 –	44	VDA0 –	RedMSB0 –
5	VDA5 +	RedMSB5 +	45	VDA1 +	Red MSB1 +
6	VDA5 –	RedMSB5 –	46	VDA1 –	RedMSB1 –
7	VDA6 +	RedMSB6 +	47	VDA2 +	RedMSB2 +
8	VDA6 –	RedMSB6 –	48	VDA2 –	RedMSB2 –
9	VDA7 +	RedMSB7 +	49	VDA3 +	RedMSB3 +
10	VDA7 –	RedMSB7 –	50	VDA3 –	RedMSB3 –
11	VDB4 +	GrnMSB4 +	51	VDB0 +	GrnMSB0 +
12	VDB4 –	GrnMSB4 –	52	VDB0 –	GrnMSB0 –
13	VDB5 +	GrnMSB5 +	53	VDB1 +	GrnMSB1 +
14	VDB5 –	GrnMSB5 –	54	VDB1 –	GrnMSB1 –
15	VDB6 +	GrnMSB6 +	55	VDB2 +	GrnMSB2 +
16	VDB6 –	GrnMSB6 –	56	VDB2 –	GrnMSB2 –
17	VDB7 +	GrnMSB7 +	57	VDB3 +	GrnMSB3 +
18	VDB7 –	GrnMSB7 –	58	VDB3 –	GrnMSB3 –
19	VDA8 +	BluMSB0 +	59	VDB8 –	BluMSB0 –
20	+5V	Not used	60	+5V	Not used
21	VDA10 +	AMSB10 +	61	VDA10 –	AMSB10 –
22	VDA11 +	BluMSB4 +	62	VDA11 –	BluMSB4 –
23	Ground	Not used	63	Ground	Not used
24	SCNTLO +	Serial Control Out +	64	PSTRB +	Pixel Strobe +
25	SCNTLO –	Serial Control Out –	65	PSTRB –	Pixel Strobe –
26	VDB10 +	BluMSB6 +	66	LINE +	Line Enable +
27	VDB10 –	BluMSB6 –	67	LINE –	Line Enable –
28	ID1 +	BluMSB7 +	68	FRME +	Frame Enable +
29	ID1 –	BluMSB7 –	69	FRME –	Frame Enable –
30	Spare7 +	Not used	70	VDB11 +	BluMSB5 +
31	Spare7 –	Not used	71	VDB11 –	BluMSB5 –
32	SCNTLI +	Serial Control In +	72	VDA9 +	BluMSB1 +
33	SCNTLI –	Serial Control In –	73	VDA9 –	BluMSB1 –
34	Spare13 +	Not used	74	VDB8 +	BluMSB2 +
35	Spare13 –	Not used	75	VDB8 –	BluMSB2 –
36	Spare14 +	Not used	76	VDB9 +	BluMSB3 +
37	Spare14 –	Not used	77	VDB9 –	BluMSB3 –
38	EXPOSEB +	FRMRST/EXP +	78	EXPOSE +	Not used
39	EXPOSEB –	FRMRST/EXP –	79	EXPOSE –	Not used
40	Ground	Ground	80	Ground	Ground

Table 3. PCI DV for Single-channel Color Cameras

Shading denotes out to camera.

PCI DVK Pin	PCI DVK Signal	AIA Signal	PCI DVK Pin	PCI DVK Signal	AIA Signal
1	Ground	Ground	35	Ground	Ground
2	VD0 +	MSB +	36	VD0 –	MSB –
3	VD1 +	MSB1 +	37	VD1 –	MSB1 –
4	VD2 +	MSB2 +	38	VD2 –	MSB2 –
5	VD3 +	MSB3 +	39	VD3 –	MSB3 –
6	VD4 +	MSB4 +	40	VD4 –	MSB4 –
7	VD5 +	MSB5 +	41	VD5 –	MSB5 –
8	VD6 +	MSB6 +	42	VD6 –	MSB6 –
9	VD7 +	MSB7 +	43	VD7 –	MSB7 –
10	VD8 +	MSB8 +	44	VD8 –	MSB8 –
11	VD9 +	MSB9 +	45	VD9 –	MSB9 –
12	Spare7 +	Ground	46	Spare7 –	Ground
13	VD10 +	MSB10 +	47	VD10 –	MSB10 –
14	VD11 +	MSB11 +	48	VD11 –	MSB11 –
15	VD12 +	MSB12 +	49	VD12 –	MSB12 –
16	VD13 +	MSB13 +	50	VD13 –	MSB13 –
17	Spare17 +	Not used	51	Spare17 –	Not used
18	Spare18 +	Not used	52	Spare18 –	Not used
19	VD14 +	MSB14 +	53	VD14 –	MSB14 –
20	VD15 +	MSB15 +	54	VD15 –	MSB15 –
21	Spare16 +	Reserved	55	Spare16 –	Reserved
22	SCNTLO +	Serial Control Out +	56	SCNTLO –	Serial Control Out –
23	SCNTLI +	Serial Control In +	57	SCNTLI –	Serial Control In –
24	FLDID +	Field ID +	58	FLDID –	Field ID –
25	FRME +	Frame Enable +	59	FRME –	Frame Enable –
26	LINE +	Line Enable +	60	LINE –	Line Enable –
27	ID0 +	Channel ID 0 +	61	ID0 –	Channel ID 0 –
28	ID1 +	Channel ID 1 +	62	ID1 –	Channel ID 1 –
29	PSTRB +	Pixel Strobe +	63	PSTRB –	Pixel Strobe –
30	EXPOSE +	Mode Control 0 +	64	EXPOSE –	Mode Control 0 –
31	MC0 +	Mode Control 1 +	65	MC0 –	Mode Control 1 –
32	MC1 +	Mode Control 2 +	66	MC1 –	Mode Control 2 –
33	MC2 +	Mode Control 3 +	67	MC2 –	Mode Control 3 –
34	Ground	Ground	68	Ground	Ground

Table 4. PCI DVK for Single-channel Grayscale Cameras

Shading denotes out to camera.

PCI DVK Pin	PCI DVK Signal	AIA Signal	PCI DVK Pin	PCI DVK Signal	AIA Signal
1	Ground	Ground	35	Ground	Ground
2	VDA0 +	AMSB +	36	VDA0 –	AMSB –
3	VDA1 +	AMSB1 +	37	VDA1 –	AMSB1 –
4	VDA2 +	AMSB2 +	38	VDA2 –	AMSB2 –
5	VDA3 +	AMSB3 +	39	VDA3 –	AMSB3 –
6	VDA4 +	AMSB4 +	40	VDA4 –	AMSB4 –
7	VDA5 +	AMSB5 +	41	VDA5 –	AMSB5 –
8	VDA6 +	AMSB6 +	42	VDA6 –	AMSB6 –
9	VDA7 +	AMSB7 +	43	VDA7 –	AMSB7 –
10	VDB0 +	BMSB +	44	VDB0 –	BMSB –
11	VDB1 +	BMSB1 +	45	VDB1 –	BMSB1 –
12	Spare7 +	Ground	46	Spare7 –	Ground
13	VDB2 +	BMSB2 +	47	VDB2 –	BMSB2 –
14	VDB3 +	BMSB3 +	48	VDB3 –	BMSB3 –
15	VDB4 +	BMSB4 +	49	VDB4 –	BMSB4 –
16	VDB5 +	BMSB5 +	50	VDB5 –	BMSB5 –
17	Spare17 +	Not used	51	Spare17 –	Not used
18	Spare18 +	Not used	52	Spare18 –	Not used
19	VDB6 +	BMSB6 +	53	VDB6 –	BMSB6 –
20	VDB7 +	BMSB7 +	54	VDB7 –	BMSB7 –
21	VDA8 +	AMSB8 +	55	VDA8 –	AMSB8 –
22	SCNTLO +	Serial Control Out +	56	SCNTLO –	Serial Control Out –
23	SCNTLI +	Serial Control In +	57	SCNTLI –	Serial Control In –
24	FLDID +	Field ID +	58	FLDID –	Field ID –
25	FRME +	Frame Enable +	59	FRME –	Frame Enable –
26	LINE +	Line Enable +	60	LINE –	Line Enable –
27	ID0 +	Channel ID 0 +	61	ID0 –	Channel ID 0 –
28	ID1 +	Channel ID 1 +	62	ID1 –	Channel ID 1 –
29	PSTRB +	Pixel Strobe +	63	PSTRB –	Pixel Strobe –
30	EXPOSE +	EXPOSE 0 +	64	EXPOSE –	EXPOSE –
31	VDA9 +	AMSB9 +	65	VDA9 –	AMSB9 –
32	VDB8 +	BMSB8 +	66	VDB8 –	BMSB8 –
33	VDB9 +	BMSB9 +	67	VDB9 –	BMSB9 –
34	Ground	Ground	68	Ground	Ground

Table 5. PCI DVK for Dual-channel Grayscale Cameras

Shading denotes out to camera.

PCI DVK Pin	PCI DVK Signal	AIA Signal	PCI DVK Pin	PCI DVK Signal	AIA Signal
1	Ground	Ground	35	Ground	Ground
2	VDR0 +	RedMSB0 +	36	VDR0 –	RedMSB0 –
3	VDR1 +	Red MSB1 +	37	VDR1 –	RedMSB1 –
4	VDR2 +	Red MSB2 +	38	VDR2 –	Red MSB2 –
5	VDR3 +	Red MSB3 +	39	VDR3 –	Red MSB3 –
6	VDR4 +	Red MSB4 +	40	VDR4 –	Red MSB4 –
7	VDR5 +	Red MSB5 +	41	VDR5 –	Red MSB5 –
8	VDR6 +	Red MSB6 +	42	VDR6 –	Red MSB6 –
9	VDR7 +	Red MSB7 +	43	VDR7 –	Red MSB7 –
10	VDG0 +	GrnMSB0 +	44	VDG0 –	GrnMSB0 –
11	VDG1 +	GrnMSB1 +	45	VDG1 –	GrnMSB1 –
12	Ground	Ground	46	Ground	Ground
13	VDG2 +	GrnMSB2 +	47	VDG2 –	GrnMSB2 –
14	VDG3 +	GrnMSB3 +	48	VDG3 –	GrnMSB3 –
15	VDG4 +	GrnMSB4 +	49	VDG4 –	GrnMSB4 –
16	VDG5 +	GrnMSB5 +	50	VDG5 –	GrnMSB5 –
17		not used	51		not used
18	VDB4 +	BluMSB4 +	52	VDB4 –	BluMSB4 –
19	VDB6 +	GrnMSB6 +	53	VDB6 –	GrnMSB6 –
20	VDB7 +	GrnMSB7 +	54	VDB7 –	GrnMSB7 –
21	VDB0 +	BluMSB0 +	55	VDB0 –	BluMSB0 –
22	SCNTLO +	Serial Control Out +	56	SCNTLO –	Serial Control Out –
23	SCNTLI +	Serial Control In +	57	SCNTLI –	Serial Control In –
24	VDB5 +	BluMSB5 +	58	VDB5 –	BluMSB5 –
25	FRME +	Frame Enable +	59	FRME –	Frame Enable –
26	LINE +	Line Enable +	60	LINE –	Line Enable –
27	VDB6 +	BluMSB6 +	61	VDB6 –	BluMSB6 –
28	VDB7 +	BluMSB7 +	62	VDB7 –	BluMSB7 –
29	PSTRB +	Pixel Strobe +	63	PSTRB –	Pixel Strobe –
30	EXPOSE +	EXPOSE +	64	EXPOSE –	EXPOSE –
31	VDB1 +	BluMSB1 +	65	VDB1 –	BluMSB1 –
32	VDB2 +	BluMSB2 +	66	VDB2 –	BluMSB2 –
33	VDB3 +	BluMSB3 +	67	VDB3 –	BluMSB3 –
34	Ground	Ground	68	Ground	Ground

Table 6. PCI DVK for Single-channel Color Cameras

Shading denotes out to camera.

DVC Pin	DVC Name	PCI DV 44 Name
*1	PIXCLK +	PSTRB –
2	Ground	Ground
3	ENF +	FRME +
4	MSB +	VD0 +
5	MSB1 +	VD1 +
6	MSB2 +	VD2 +
7	MSB3 +	VD3 +
8	MSB4 +	VD4 +
9	MSB5 +	VD5 +
10	MSB6 +	VD6 +
11	MSB7 +	VD7 +
12	MSB8 +	VD8 +
13	MSB9 +	VD9 +
14	MSB10 +	VD10 +
15	MSB11 +	VD11 +

DVC Pin	DVC Name	PCI DV 44 Name
*16	PIXCLK –	PSTRB +
17	Ground	Ground
18	ENF –	FRME –
19	MSB –	VD0 –
20	MSB1 –	VD1 –
21	MSB2 –	VD2 –
22	MSB3 –	VD3 –
23	MSB4 –	VD4 –
24	MSB5 –	VD5 –
25	MSB6 –	VD6 –
26	MSB7 –	VD7 –
27	MSB8 –	VD8 –
28	MSB9 –	VD9 –
29	MSB10 –	VD10 –
30	MSB11 –	VD11 –

DVC Pin	DVC Name	PCI DV 44 Name
31	ENL +	LINE +
32	ENL –	LINE –
33	Not used	
34	INPUT1 +	EXPOSE +
35	INPUT1 –	EXPOSE –
**36	R1 IN	SCNTLI
**37	T1 OUT	SCNTLO
38	COM GND	Ground
39	VRST_INT	Not used
40	Reserved	MC2 +
41	Ground	Ground
42	Reserved	MC2 –
43	Ground	Ground
44	Reserved	Not used

Table 7. PCI DV44 for DVC1310 and DVC1312 Cameras

Shading denotes out to camera.

Other DVC1300 series cameras may have a different pinout and would therefore not be compatible with the PCI DV 44.

* Cable is straight through, except that wires for PSTRB + and PSTRB – are swapped.

** SCNTLI and SCNTLO are single-ended RS232 signals; all others are LVDS signal pairs.

Registers

Xilinx Programmable Gate Array Registers

The EDT software driver on the host computer uses the following registers (implemented in the Xilinx field-programmable gate array) to control the camera.

Note If you're not writing your own driver for the PCI DV, skip these implementation details.

As the camera data passes through the Xilinx, the firmware performs various operations on it, in the following order. Use the registers described below to affect the data pipeline as follows:

1. Apply the region-of-interest counters if region of interest is enabled in the ROI Control register.
2. If the SWAP_FOR_AIA bit is true in the Shift register, the firmware swaps the 16-bit camera data end for end, so that bit 0 becomes bit 15, bit 1 becomes bit 14, and so on. AIA style cameras place the MSB on VD[0], many non-AIA cameras place the LSB on VD[0].
3. Barrel-shift the 16-bit camera data 0 to 15 places, as determined by the four least significant bits of the Shift register.
4. If the INVERT_DATA bit is true in the Data Path register, invert the data.
5. Zero any bits for which the 16-bit Mask registers have a value of 0.
6. If the EXT_DEPTH bit of the Data Path register is 0, then only bits 0–7 are sent to the host as a single byte; bits 8–15 are ignored.
7. If the BSWAP bit of the Utility register is true, swap even and odd bytes of each 16-bit word.
8. If the SSWAP bit of the Utility register is true, swap even and odd 16-bit words of each 32-bit word.

Table 8 lists the PCI DV registers implemented with AIA firmware. Each register or set of registers is described in the following sections.

Register	Address(es)	Size (in bits)	Read/Write
Command	0x00	8	write-only
Status	0x01	8	read-only
Configuration	0x02	8	write-only
Shutter	0x03	8	write-only
Shutter Time Left	0x03	8	read-only
Polarity Select	0x05	8	read-write
Data Path	0x06	8	read-write
Mode Control	0x07	8	read-write
Video Data Lo	0x08	8	read-write
Video Data Hi	0x09	8	read-write
Serial Data	0x0A	8	read-write
Serial Data Status	0x0B	8	read-write
Serial Data Control	0x0C	8	read-write
Utility	0x0F	8	read-write
Utility2	0x10	8	read-write
Shift	0x11	8	read-write
Mask Lo	0x12	8	read-write
Mask Hi	0x13	8	read-write
Region of Interest Control	0x17	8	read-write
Horizontal Skip Lo	0x18	8	write-only
Horizontal Skip Hi	0x19	8	write-only
Horizontal Active Lo	0x1A	8	write-only
Horizontal Active Hi	0x1B	8	write-only
Vertical Skip Lo	0x1C	8	write-only
Vertical Skip Hi	0x1D	8	write-only
Vertical Active Lo	0x1E	8	write-only
Vertical Active Hi	0x1F	8	write-only
Frame Rate Counter	0x20, 0x21, 0x22, 0x23	8	read-write
Status2	0x35	8	read-write

Table 8. PCI DV Registers

Device Control Registers

Command Register

Size 8-bit

I/O write-only

Address 0x00

Comments Bits written to this register are strobe bits and need not be cleared after setting. When read, this register is the Firmware ID register, described next.

Bit	Name	Description
7	STROBE_PIXEL	For debug, setting this bit strobes one pixel of camera data (perhaps from the video data hi/lo registers) out to the host.
6-5	Not used	
4	CLRFVINT	Setting this bit clears the frame valid interrupt.
3	CLEAR_CONT	Strobe this bit to clear the CONTINUOUS bit of the Data Path register the next time that the AQUIRE_IP bit in the Status register is true. If AQUIRE_IP is true when this bit is strobed, CONTINUOUS is cleared immediately.
2	AQ_CLR	Resets AQUIRE_INT bit of serial data status register.
1	ENABLE_GRAB	Enable acquisition of the next complete frame. If enabled in the configuration register, the shutter time is started. If the continuous acquisition bit is set in the data path register, then ENABLE_GRAB starts acquisition, which continues until the continuous bit is reset.
0	RESET_INTFC	Setting this bit resets the PCI DV interface board.

Status Register

Size 8-bit

I/O read-only

Address 0x01

Comments The executable *watchstat* (included with the PCI DV software) reads and displays this register symbolically

Bit	Name	Description
7	AQUIRE_IP	When set, the camera interface has detected a valid beginning of frame and is presently acquiring data.
6	GRAB_ARMED	When set, the grab command has been issued, any specified hardware trigger has been detected, and the camera interface is waiting for a valid beginning of a frame.
5	CHAN_ID1	Reflects state of the AIA Channel Identification 1 signal.
4	CHAN_ID0	Reflects state of the AIA Channel Identification 0 signal.
3	TRIGGER_ARMED	When set, the grab command has been issued, and the board is ready for a hardware trigger. Cleared when AQUIRE_IP goes true unless the AQUIRE_MULT bit of the Utility2 register is set.
2	EXPOSURE	When set, the expose line for the camera is asserted.
1	FRAME_VALID	When set, the camera shutter has closed and valid data is being transmitted (though the PCI DV is not necessarily acquiring data).
0	OVERRUN	When set, indicates that data was lost during a frame transfer because the host was not ready to receive at the rate at which the camera was transmitting; therefore the data has been corrupted.

Configuration Register

Size 8-bit

I/O write-only

Address 0x02

Bit	Name	Description
7	INT_ENAQ	Setting this bit enables the acquisition interrupt, which occurs with the rising edge of the status register's AQUIRE_IP bit. Clear the interrupt with the command register's AQ_CLR bit.
6	EN_DALSA	Setting this bit enables DALSA mode. Maps correct signals and polarities out to MC[0-3] for controlling exposure time with PRIN and external sync on Dalsa area scan cameras.
5	Not used	
4	BAUD2	Together with bits BAUD0 and BAUD1 of the Serial Data Control register, determines the baud rate of the serial port to the camera.
3	FIFO_RESET	Set and clear this bit to reset the PCI DV input FIFO.
2	INV_SHUTTER	When set, the polarity of the shutter signal is inverted. The shutter signal is assigned to a mode control signal in the mode register. When cleared, the mode signal is positive when the shutter is open. This bit must also be set for Dalsa line scan cameras (but not area scan cameras). See the description of the EN_DALSA bit of this register.
1	TRIG	Obsolete; set to 0. Instead, set the shutter timer to the desired length of the trigger pulse, using the Shutter register and the DECADE bits of the Data Path register.
0	DIS_SHUTTER	Obsolete; set to 0. Disable the EXPOSE signal out to the camera by clearing the four most significant bits of the Mode Control register.

Shutter Register

Size 8-bit

I/O write-only

Address 0x03

Bit	Description
7-0	Specifies the exposure time –1 (time that the shutter must remain open) in increments of 1 ms, 10 ms or 100 ms: the time base is selected by the DECADE bits in the data path register. If the time base is 1 ms, write 2 for a 3 ms exposure, 3 for a 4 ms exposure, and so on. If the time base is 10 ms, write 2 for a 30 ms exposure.

Shutter Time Left Register

Size 8-bit

I/O read-only

Address 0x03

Comments When written, this is the Shutter register, described above

Bit	Description
7-0	Specifies the amount of time left before the current exposure terminates.

Polarity Select Register

Size 8-bit

I/O read-write

Address 0x05

Bit	Name	Description
7	FRENA	Enables constant frame-rate mode. See Frame Rate Counter Registers on page 36 for more information.
6	FVADJ	Adjusts length of frame valid for holding off next frame. See Frame Rate Counter Registers on page 36 for more information.
5-3		Not used
2	FV_INT_POLARITY	When 1, Frame Valid interrupt occurs on rising edge of frame valid.
1	FV_INVERT	When 1, invert Frame Valid from camera.
0	LV_INVERT	When 1 invert Line Valid from camera.

Data Path Register

Size 8-bit

I/O read-write

Address 0x06

Bit	Name	Description
7-6	DECADE [1-0]	Selects the time base for the shutter counter: **DECADE1 DECADE0 Time Base** 0 0 1 millisecond 0 1 10 milliseconds 1 0 100 milliseconds 1 1 Reserved
5	Interlaced	Set if camera is interlaced. In this case, acquisition waits until the first frame valid when the Field ID signal is true.
4	CONTINUOUS	Set if PCI DV is to acquire successive frames of data. ENABLE_GRAB in the Command register must be set to start acquisition. After CONTINUOUS has been cleared, acquisition continues until the end of a complete frame. Clear in either of two ways: write 0 to this bit to clear it

		immediately, or strobe the CLEAR_CONT bit of the Command register to clear this bit after the next DMA transfer completes.
3	INVERT_DATA	Inverts the incoming data.
2-1	Not used	
0	EXT_DEPTH	Set to send 16 bits to the host for each pixel clock from the camera. Clear to send only the eight least significant bits.

Mode Control Register

Size 8-bit

I/O read-write

Address 0x07

Bit	Name	Description
7-4	EN_SHUTTER [3-0]	Selects which mode code signal is driven by the internal signal EXPOSE from the shutter timer. If all these bits are 0, no EXPOSE signal is sent to the camera. If one of these bits is asserted when in continuous mode, the shutter time asserts EXPOSE to the camera once per frame. This bit is ignored if bit 4 (ENMCOUTL) is set in the Utility register.
3-0	AIA_MC[3-0]	If the output is not enabled as a shutter with the EN_SHUTTER bits above, sets the state of the camera control outputs.

Video Data Lo Register

Size 8-bit

I/O read-write

Address 0x08

Bit	Name	Description
7-0	VD[7-0]	Data written to this register is driven out on the 8 data signal pairs to the camera if the VID_DIRECTION bit of the Utility register is 1. When read, it shows the current state of those 8 lines. Note that VD[0] is the least significant bit of this register, though the AIA cameras place their most significant bit on this line. (Not available in all Xilinx configuration files.)

Video Data Hi Register

Size 8-bit

I/O read-write

Address 0x09

Bit	Name	Description
7-0	VD[15-8]	Data written to this register is driven out on the 8 data signal pairs to the camera if the VID_DIRECTION bit of the Utility register is 1. When read, it shows the current state of those 8 lines. (Not available in all Xilinx configuration files.)

The following three registers implement an asynchronous UART in the Xilinx for communicating with the camera.

Note The transmit and receive data lines to the camera are RS-422 diffferential, no RS-232 levels. Not all cameras use this serial communications channel.

Note The serial control lines are fixed at 8 data bits, one stop bit, no parity. The default baud rate is 9600 baud; you can change this using the Serial Data Control register (see page 25).

Serial Data Register

Size 8-bit

I/O read-write

Address 0x0A

Bit	Name	Description
7-0	SERIAL_DATA[0-7]	Data written to this register is output on the Serial Control Out signal if the TRANSMIT_RDY bit is set. Data read from this register reflects the last character received when the RECEIVE_RDY bit is set. (See the serial data status register below for descriptions of these bits.)

Serial Data Status Register

Size 8-bit

I/O read-write

Address 0x0B

Bit	Name	Description
7	INTFC_INT	INTFC_INT is set when the following boolean expression is true: (TRANSMIT_RDY and EN_TX_INT) or (RECEIVE_RDY and EN_RX_INT) or (AQUIRE_INT) or (FVINT). This expression is then anded with the EN_GLOB_INT bit of the serial data control register and the result passed on to the PCI Xilinx. If the RMT_EN_INTR and PCI_EN_INTR bits of the PCI interrupt and remote Xilinx configuration register in the PCI Xilinx are set (described in the PCIDV user's guide), then an interrupt is asserted over the PCI bus to the host computer.
6	FVINTSTAT	Set when a falling edge frame valid has been detected; cleared by CLRFVINT.
5	AQUIRE_INT	Set when an acquisition interrupt is enabled through the INT_ENAQ bit of the configuration register, and a rising edge of the AQUIRE_IP bit in the status register has been detected. Clear this interrupt using the AQ_CLR bit of the command register.

4	FVINT	Set when frame valid interrupt is enabled through the ENFVINT bit of the utility 2 register, and FVINTSTAT is true. Clear this interrupt using the CLRFVINT in the command register.
3–2	Not used	
1	TRANSMIT_RDY	Set when the transmitter is enabled and the holding register is ready for the next character.
0	RECEIVE_RDY	Set when the receiver is enabled and a character is available for reading.

Serial Data Control Register

Size 8-bit

I/O read-write

Address 0x0C

Bit	Name	Description
7-6	BAUD[1-0]	Select serial port baud rate for the serial data: **Bit 7** **Bit 6** **Baud Rate** 0 0 9600 0 1 19200 1 0 38400 1 1 115200
5	CL_RECEIVE_RDY	Set this bit to clear the RECEIVE_RDY bit in the Serial Data Status register.
4	EN_GLOB_INT	Global interrupt enable. Enables all interrupts.
3	EN_TX_INT	Enables the TRANSMIT_RDY interrupt.
2	EN_RX_INT	Enables the RECEIVE_RDY interrupt.
1	EN_TX	Enables the serial data transmitter.
0	EN_RX	Enables the serial data receiver.

Utility Register

Size 8-bit

I/O read-write

Address 0x0F

Bit	Name	Description
7	VID_DIRECTION	When 1, drive data from PCI DV to the camera over the video data signal pairs. Data value determined by contents of the registers video data hi and video data lo. (Not available with some Xilinx configuration files.)
6	SKIP_X	When 1, skip every other pixel in X to scale image down by 2.
5	Not used	
4	ENMCOUTL	A value of 0 enables Mode Control output; a value of 1 disables it, allowing the four signal pairs labeled MC[0-3] to be used for incoming data. In this case, values set in the Mode Control register are ignored.
3	SSWAP	A value of 1 swaps the order of 16-bit shorts in a 32-bit word of data coming in from the camera, to accommodate host computer byte order.
2-1	PAD[1-0]	Append 0 to 3 extra pixels at the end of each raster. Use to achieve an even number of 32-bit words per raster to optimize processing of the camera data by the host. For the special Cincinnati Electronics Xilinx configuration file, when PAD0 is set, every 161st pixel is discarded, yielding 160 pixels per raster on the IRRIS160ST. PAD1 is ignored.
0	BSWAP	A value of 1 swaps the order of bytes in a 16-bit word of data coming in from the camera, to accommodate host computer byte order.

Hardware Triggering

By default, the EDT camera interface grabs a single frame from the camera each time the application program strobes the START bit in the Command register.

If the Continuous bit in the Data Path register is set, the EDT camera interface grabs frames continuously as fast as possible. This action starts after the START bit is strobed.

Hardware triggering provides additional flexibility. Nothing happens until the START bit is strobed (same as before); but acquisition is delayed until a hardware trigger is received. The interface can be configured for a single frame, or one frame for each hardware trigger, or to be continuous after a trigger.

The source of the hardware trigger is typically from the optical isolator on the EDT camera interface board.

Some EDT products allow the FIELDID signal to serve as a hardware trigger. This signal is not used on most non-interlaced cameras. (The PCI DV CL uses the SERTFG signal on Camera Link cable 2 as the source of FIELDID for hardware triggering.)

A third source for the hardware trigger is a constant frame rate signal generated by counters inside the FPGA on the EDT camera interface board.

In the following table, the Continuous bit is found in the Data Path register; the three HWtrig bits are found in the Utility2 register. Action taken on bit combinations not shown is not defined.

CONTINUOUS	HWTRIG2	HWTRIG1	HWTRIG0	Description
0	0	0	0	Acquire next single frame from camera.
0	0	0	1	Wait for trigger via optical isolator, then acquire a single frame from the camera.
0	0	1	0	Wait for trigger from FIELDID signal, then acquire one frame.
1	0	0	0	Acquire data continuously from camera.
1	0	0	1	Acquire a frame of data for each optical isolator trigger.
1	0	1	0	Acquire a frame of data for each FIELDID trigger.
1	1	0	1	Wait for trigger from optical isolator, then acquire data continuously from the camera.
1	1	1	0	Wait for trigger from FIELDID, then acquire data continuously from the camera.

CONTINUOUS	HWTRIG2	HWTRIG1	HWTRIG0	Description
1	0	1	1	Acquire data continuously from the camera at the rate determined by the Frame Rate counters.
1	1	1	1	Acquire data continuously from the camera at the rate determined by the Frame Rate counters, but only after a trigger from the optical isolator.

Table 9. Hardware Triggering

To use HWTRIGEN_OPTO (the optical coupler) for the hardware trigger source, call EDT and ask for the optical coupler PCI panel. It uses a standard female DB9 connector. Drive the signal into pins 2 and 3 at 5 V, 10 mA; either polarity is acceptable.

To use HWTRIGEN_FLDID (the field ID pins) for the hardware trigger source, drive an EIA-644 (or RS-422, if applicable) differential signal into pins 70 (+) and 71 (–) of the camera connector for the PCI DV (pins 24 (+) and 58 (–) for the PCI DVK).

Utility2 Register

Size 8-bit

I/O read-write

Address 0x10

Comments The ENABLE_GRAB bit in the Command register arms the interface for a single hardware trigger. If no hardware trigger is enabled, then the Xilinx triggers immediately and grabs the next frame of data from the camera. If OPTO_TRIGGER is enabled, then the Xilinx waits until a trigger is received through the optical isolator instead. If FIELDID_TRIGGER is true, then the Xilinx waits until a trigger is received from the FIELDID differential pair. If you are using an interlaced camera, the FIELDID pair is not available for this use.

Once triggered, the Xilinx ordinarily acquires a single frame; if the CONTINUOUS bit is set in the Data Path register, then a single trigger grabs all subsequent frames from the camera.

Bit	Name	Description
7	SELECT_MC4	Setting SELECT_MC4 causes the differential pair normally assigned to SCNTLO (Serial Control Out) to be used instead as a fifth mode control bit.
6	MC4	A fifth mode control bit, used by some Photonics cameras as the Photonics SELECT line.
5	PULNIX	True for all Pulnix cameras. Allows EXPOSE to camera to be asserted even when the incoming FRAME VALID line is true; waits till the end of EXPOSE before GRAB_ARMED (bit 6 of the Status register) goes true.
4	DBL_TRIG	Enable double trigger mode on the EXPOSE signal out to the camera. Used for some Pulnix model cameras.
3	Not used	
2-0	HWTRIG[2-0]	Selects mode of operation for hardware triggering as described in Table 7.

Shift Register

Size 8-bit

I/O read-write

Address 0x11

Comments The default state of 0 causes all 16 bits of camera data to pass through unchanged.

Bit	Name	Description
7-6	Not used	
5	MARK09	When true, forces a 1 on bits 0 and 9 of the 16-bit data path after the mask has been applied. The driver can use this to determine how the host orders bytes during DMA. See following Determining Host Byte Order section.
4	SWAP_FOR_AIA	When true, the incoming 16-bit camera data is swapped end for end (bit 0 becomes bit 15, bit 14 becomes 1, etc.)
3-0	SHIFT[3-0]	A shift value of 0-15, determining how many places to barrel-shift incoming data downward. For example, a value of 4 moves bits 4-15 down to bits 0-11 (and bits 0-3 around to bits 15-12 where they may subsequently be masked off), suitable for many 12-bit cameras.

Determining Host Byte Order

The PCI Bus is little-endian. Big-endian hosts sometimes swap byte order during DMA to accommodate the PCI Bus. To determine host byte order:

1. Clear the BSWAP and SSWAP bits of the Utility register.
2. Clear the Mask Lo and Mask Hi registers.
3. Use the STROBE_PIXEL bit of the Command register to strobe any 16-bit word into the DMA pipeline. (It will be masked out by the zeroes in the Mask registers.)
4. Set the MARK09 bit of the Shift register (above); the values of all other bits are irrelevant.
5. Use the STROBE_PIXEL bit of the Command register to strobe another 16-bit word into the DMA pipeline.
6. Have the host perform a DMA read operation of one 32-bit word from the PCI DV.
7. The correct little-endian byte stream for this word is 0x00 0x00 0x01 0x02 (the bits forced to one by the MARK09 bit, above). Determine your result and, if necessary, adjust the BSWAP and SSWAP bits of the Utility register to compensate as required.

Mask Lo Register

Size 8-bit

I/O read-write

Address 0x12

Bit	Name	Description
7-0	MASK[7-0]	Bits that are 0 force the corresponding camera data bit to 0.

Mask Hi Register

Size 8-bit

I/O read-write

Address 0x13

Bit	Name	Description
7-0	MASK[15-8]	Bits that are 0 force the corresponding camera data bit to 0.

Region of Interest

Some PCI DV boards support a region of interest, a rectangle you can define to crop an image horizontally and vertically, thus eliminating superfluous pixels. To determine whether your board supports this capability:

Write a 0 to the Region of Interest Control register.

Read the register back. The value returned specifies whether region of interest is supported:

0x00	Region of interest, simulator, Dalsa line scan, and dual channel cameras supported.
0x80	Region of interest, simulator, Dalsa line scan, and dual channel cameras **not** supported.
0xC4	Region of interest, simulator, Dalsa line scan, and dual channel cameras **not** supported; special Xilinx gate array configuration for Irris 256ST and 160ST camera models.
Other values	Undefined.

Note If Region of Interest is not supported, the only part of the ROI Control register available is the bottom three bits, which set the pixel clock rate.

The region of interest registers are 8-bit write-only registers; each set of two stores a 16-bit integer. Assuming region of interest is enabled, the region of interest registers specify the size of the region of interest as described below. The examples that follow assume a 1024 x 1024 image with a 10-pixel border on all four sides that you wish to crop; thus, a region of interest that is 1004 x 1004.

If you set the SIM_SYNC bit in the ROI Control register, thus enabling simulator mode, and you then write a value to the region of interest registers, the Horizontal and Vertical Skip registers determine the amount of time spent in horizontal and vertical blanking, respectively, and the Horizontal and Vertical Active registers cause the PCI DV to acquire same number of pixels as would be the case if you'd set the ROI_EN bit, thus enabling region of interest.

If you've enabled Dalsa line scan mode by setting the DALSA_LS bit, the period of the EXTSYNC pulse generated is determined by sum of the Horizontal Skip and Horizontal Active pixel counts. The amount of time that PRIN is asserted is determined by the value in the Horizontal Skip registers. If region of interest is also enabled, the vertical counters are used to determine how many rasters to skip and how many rasters to acquire.

For more information about EXTSYNC and PRIN, see the Dalsa documentation.

Region of Interest (ROI) Control Register

Size 8-bit

I/O read-write

Address 0x17

Comments Besides enabling or disabling a region of interest, use this register to enable or disable Dalsa line scan mode and simulator mode. These bits are not all independent; in particular, simulator mode requires compatible settings. You can run with simulated data (bit 4 true) using either internal or camera timing (bit 5 true or false), but if bit 5 is true, enabling internal timing, you must also set bit 4 true to use simulated data; otherwise, you will see random pixel data from the camera, as the data and timing will be unsynchronized.

Simulted data is generated as follows:

Data bits 0-7 receive the eight least significant bits of the horizontal pixel count. Bit 7 is inverted once each frame. The data at the start of each raster begins with a value of –2 (0xFE) and counts up. Data bits 8-15 receive the eight least significant bits of the vertical line count, starting with 0x00 and count up.

Simulted data has the least significant bit in data bit 0; therefore, do not set the SWAP_FOR_AIA bit of the Shift register when using the simulator.

Bit	Name	Description
7	DALSA_LS	A value of 1 (true) indicates Dalsa line scan mode, in which the horizontal window registers are used to determine the timing of the EXTSYNC and PRIN lines out to the Dalsa camera. If region of interest is also enabled (see bit 6), the region of interest affects only the number of lines per frame as determined by the vertical window registers; the number of pixels per raster is always as specified by the Dalsa camera.
6	ROI_EN	A value of 1 (true) enables region of interest mode, allowing you to crop the image to a rectangular region of interest. The camera transfers to the host only those pixels in the region of interest, as specified by the Region of Interest registers.

5	SIM_SYNC	A value of 1 (true) indicates simulator mode. A simulated image of the size specified by the Region of Interest registers is generated automatically, as if from a camera. To run in simulator mode, also set the SIM_DAT bit to true, and the ROI and DALSA_LS bits to false (0). The pixel clock for the simulator can be either internal or external, as determined by the PCLKSEL bits 2-0.
4	SIM_DAT	A value of 1 (true) indicates that simulated data comes from the Region of Interest register counters rather than from the camera. You can use simulated data with or without the SIM_SYNC (simulated timing) and PCLKSEL bits.
3	DUAL_CHAN	Set to 1 to enable a data path suitable for dual-channel cameras. Available only for boards that support region of interest capability.
2-0	PCLKSEL	Determines the speed of the clock for the pixel data path.

Bit 2	**Bit 1**	**Bit 0**	**Pixel Clock Rate**
0	0	0	from camera
0	0	1	double rate from camera
0	1	0	undefined
0	1	1	undefined
1	0	0	20 MHz
1	0	1	10 MHz
1	1	0	5 MHz
1	1	1	undefined

Horizontal Skip Lo and Horizontal Skip Hi Registers

Size 8-bit

I/O write-only

Address 0x18 and 0x19

Comments Load these registers with a 16-bit integer specifying the number of pixels to skip at the start of each line. For example, to skip the first 10 pixels of each line, load these registers with the 16-bit value 0x000A.

Bit	Name	Description
7-0	HSKIP[7-0]	Number of pixels to crop at start of each line.

Bit	Name	Description
7-0	HSKIP[15-8]	Number of pixels to crop at start of each line.

Horizontal Active Lo and Horizontal Active Hi Registers

Size 8-bit

I/O write-only

Address 0x1A and 0x1B

Comments Load these registers with a 16-bit integer specifying the number of pixels to transfer minus 1, on each line, after the blank pixels have been skipped (as specified in Horizontal Skip registers). For example, to acquire 1004 pixels per line, load these registers with 0x03EB.

Bit	Name	Description
7-0	HACT[7-0]	[number of pixels to transfer]-1 on each line, after blank pixels are skipped.

Bit	Name	Description
7-0	HACT[15-8]	[number of pixels to transfer]-1 on each line, after blank pixels are skipped.

Vertical Skip Lo and Vertical Skip Hi Registers

Size 8-bit

I/O write-only

Address 0x1C and 0x1D

Comments Load these registers with a 16-bit integer specifying the number of lines (rasters) to skip at the start of each frame. For example, to skip the first 10 lines of each frame, load these registers with the 16-bit value 0x000A.

Bit	Name	Description
7-0	VSKIP[7-0]	Number of lines to crop at start of each frame.

Bit	Name	Description
7-0	VSKIP[15-8]	Number of lines to crop at start of each frame.

Vertical Active Lo and Vertical Active Hi Registers

Size 8-bit

I/O write-only

Address 0x1E and 0x1F

Comments Load these registers with a 16-bit integer specifying the number of lines (rasters) to transfer minus 1, on each line, after the blank lines have been skipped (as specified in Vertical Skip registers). For example, to acquire 1004 lines per frame, load these registers with 0x03EB.

Bit	Name	Description
7-0	VACT[7-0]	[number of lines to transfer]-1 for each frame, after blank lines are skipped.

Bit	Name	Description
7-0	VACT[15-8]	[number of lines to transfer]-1 for each frame, after blank lines are skipped.

Frame Rate Counter Registers

Size	8-bit
I/O	read-write
Address	0x14, 0x15, 0x16
Comments	Load these registers with a 24-bit integer specifying the frame rate in µs. For a constant frame rate of N µs, preload these registers with N -2. Normally, a grab from the camera is initiated by asserting the ENABLE_GRAB bit of the Control register. This will cause the EXPOSE line out to the camera to be asserted for the period of time specified by the shutter timer register. Once EXPOSE is finished, the camera will transfer the frame of data, asserting FRAME-VALID while sending the data. Once the transfer is complete, the interface is ready to start the entire process over again for the next grab. Bits 6 (FVADJ) and 7 (FRENA) of the Polarity Select register determine how the Frame Rate Counter gets used (do not set both). See page 21 for more information about the Polarity Select register. When the control bits FVADJ and FRENA are both zero, the Frame Rate Counter registers have no effect, and the interface operates as described above. When bit FRENA is set, the camera is triggered and a frame of camera data is grabbed at a constant frame rate, as determined by the contents of the three frame rate counter registers. (There is no need to strobe ENABLE_GRAB in the Control register.) When bit FRADJ is set, everything works as it would otherwise except that a special version of the camera's FRAME-VALID signal is generated inside the EDT interface, called FRATE-FRAME-VALID. This new signal is used to determine when a previous frame is complete enough that the next frame can be started. The new signal FRATE-FRAME-VALID turns on at the same time as FRAME-VALID from the camera, but then turns off only after the number of microseconds specified in the Frame Rate registers. Some cameras are not ready for the next EXPOSE signal until some time after the previous frame is complete. For these cameras you need to set the Frame Rate Counter registers for a value in microseconds that is longer than the actual FRAME-VALID signal from the camera.

frame is still being transferred to the EDT interface. For these cameras you may set the Frame Rate Counter registers to a value in microseconds that is less than the actual FRAME-VALID signal from the camera.

Operation when both FVADJ and FRENA are set is undefined.

Frame Rate Counter Lo

Bit	Name	Description
7-0	FRATE[7-0]	Frame rate in milliseconds.

Frame Rate Counter Mid

Bit	Name	Description
7-0	FRATE[15-8]	Frame rate in milliseconds.

Frame Rate Counter Hi

Bit	Name	Description
7-0	FRATE[23-16]	Frame rate in milliseconds.

Status2 Register

Size 8-bit

I/O read-write

Address 0x35

Bit	Name	Description
7–5		Not used
4	TRIGES40	Special trigger signal from Roper ES 4.0 camera (not normally used).
3–2		Not used
1	WTRIG	Status of incoming trigger on FIELDID signal pair.
0	PTRIG	Status of incoming trigger on optical isolator.

References

Automated Vision Components – Cameras – AIA Monochrome Digital Interface Specification, document # BSR/AIA A15.08/3-199X, available from:

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