

PCI DV FCI USPS

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Overview

The USPS firmware is an alternative to the standard AIAG firmware installed on the EDT PCI DV FCI camera interface board. This firmware was developed to meet the standards set forth in the Siemens Dematic *Statement of Work for Flexible Camera Interface Version 0.5*. The PCI DV FCI board does not have a separate interface Xilinx like the PCI DVa board, so there is no need to download a bitfile such as aiag.bit. The USPS firmware is already stored in non-volatile flash when shipped.

The USPS firmware operates in three different modes: four-channel black and white (4 bits per pixel clock), two-channel grayscale (16 bits per pixel clock), and four-channel grayscale (32 bits per pixel clock).

The USPS firmware is used with linescan cameras that provide a frame valid signal covering a variable number of rasters. If an excessively long image is detected, the image is truncated to the maximum number of raster lines specified by the user.

Provisions are made to increase noise immunity by ensuring that each raster, once started, is returned with the specified number of pixels, regardless of how many pixels the camera provides. Any extra pixels are discarded; a raster too short is padded with the last valid pixel received.

When the image is complete, a final raster of status information is added to the end.

In most other respects, the USPS firmware is like the standard EDT AIAG firmware.

Electrical Signals

All signals are low voltage differential signals (LVDS) or TIA/EIA 644.

Connector Pinout

4-Channel Grayscale (Wide Field of View)

EDT Cable 016-01689-00 (10') or 016-01926-00 (15')			
Camera Signal	Camera Pin	EDT pin	EDT signal
Ground	1	1	GND
Ground	2	2	GND
+GSA0	3	9	DATA7
-GSA0	4	10	DATAL7
+GSA1	5	7	DATA6
-GSA1	6	8	DATAL6
+GSA2	7	5	DATA5
-GSA2	8	6	DATAL5
+GSA3	9	3	DATA4
-GSA3	10	4	DATAL4
+GSA4	11	49	DATA3
-GSA4	12	50	DATAL3
+GSA5	13	47	DATA2
-GSA5	14	48	DATAL2
+GSA6	15	45	DATA1
-GSA6	16	46	DATAL1
+GSA7	17	43	DATA0
-GSA7	18	44	DATAL0
+GSB0	19	17	DATA15
-GSB0	20	18	DATAL15
+GSB1	21	15	DATA14
-GSB1	22	16	DATAL14
+GSB2	23	13	DATA13
-GSB2	24	14	DATAL13
+GSB3	25	11	DATA12
-GSB3	26	12	DATAL12
+GSB4	27	57	DATA11

EDT Cable 016-01689-00 (10') or 016-01926-00 (15')			
Camera Signal	Camera Pin	EDT pin	EDT signal
-GSB4	28	58	DATAL11
+GSB5	29	55	DATA10
-GSB5	30	56	DATAL10
+GSB6	31	53	DATA9
-GSB6	32	54	DATAL9
+GSB7	33	51	DATA8
-GSB7	34	52	DATAL8
Ground	35		
Ground	36		
+GSC0	37	30	CTR7
-GSC0	38	31	CTRL7
+GSC1	39	28	CTR6
-GSC1	40	29	CTRL6
+GSC2	41	26	CTR5
-GSC2	42	27	CTRL5
+GSC3	43	24	CTR4
-GSC3	44	25	CTRL4
+GSC4	45	70	CTR3
-GSC4	46	71	CTRL3
+GSC5	47	68	CTR2
-GSC5	48	69	CTRL2
+GSC6	49	66	CTR1
-GSC6	50	67	CTRL1
+GSC7	51	64	CTR0
-GSC7	52	65	CTRL0
+GSD0	53	38	CTR15
-GSD0	54	39	CTRL15
+GSD1	55	36	CTR14
-GSD1	56	37	CTRL14
+GSD2	57	34	CTR13
-GSD2	58	35	CTRL13



EDT Cable 016-01689-00 (10') or 016-01926-00 (15')			
Camera Signal	Camera Pin	EDT pin	EDT signal
+GSD3	59	32	CTR12
-GSD3	60	33	CTRL12
+GSD4	61	78	CTR11
-GSD4	62	79	CTRL11
+GSD5	63	76	CTR10
-GSD5	64	77	CTRL10
+GSD6	65	74	CTR9
-GSD6	66	75	CTRL9
+GSD7	67	72	CTR8
-GSD7	68	73	CTRL8
Ground	69		
Ground	70		
+GSCLK	71	19	CTR16
-GSCLK	72	59	CTRL16
+GSGATCLK	73		
-GSGATCLK	74		
+GSDV	75	22	CTR18
-GSDV	76	62	CTRL18
+GSWIN	77	21	CTR17
-GSWIN	78	61	CTRL17
Ground	79		
Ground	80		
+BINA	81		
-BINA	82		
+BINB	83		
-BINB	84		
+BINC	85		
-BINC	86		
+BIND	87		
-BIND	88		
Ground	89		



EDT Cable 016-01689-00 (10') or 016-01926-00 (15')			
Camera Signal	Camera Pin	EDT pin	EDT signal
Ground	90		
+BWCLK	91		
-BWCLK	92		
+BWGATCLK	93		
-BWGATCLK	94		
+BWDV	95		
-BWDV	96		
+BWWIN	97		
-BWWIN	98		
Ground	99		
Ground	100		

Table 1. USPS 4-Channel Grayscale Pinout

4-Channel Binary

EDT Cable (TBD if necessary)			
Camera Signal	Camera Pin	EDT pin	EDT signal
Ground	1	1	GND
Ground	2	2	GND
Not used	3-79		
Ground	80		
+BINA	81	9	DATA7
-BINA	82	10	DATAL7
+BINB	83	7	DATA6
-BINB	84	8	DATAL6
+BINC	85	5	DATA5
-BINC	86	6	DATAL5
+BIND	87	3	DATA4
-BIND	88	4	DATAL4
Ground	89		
Ground	90		
+BWCLK	91	19	CTR16
-BWCLK	92	59	CTRL16
+BWGATCLK	93		
-BWGATCLK	94		
+BWDV	95	22	CTR18
-BWDV	96	62	CTRL18
+BWWIN	97	21	CTR17
-BWWIN	98	61	CTRL17
Ground	99		
Ground	100		

Table 2. USPS 4-Channel Binary Pinout

2-Channel Grayscale (Accusort)

EDT Cable 016-01961-00 (15')			
Camera Signal	Camera Pin	EDT pin	EDT signal
AData9+	1	43	DATA0
AData7+	2	47	DATA2
AData5+	3	3	DATA4
AData5-	4	4	DATAL4
AData3+	5	7	DATA6
	6		
BData9+	7	51	DATA8
BData9-	8	52	DATAL8
BData7+	9	55	DATA10
BData5+	10	11	DATA12
BData3+	11	15	DATA14
BData3-	12	16	DATAL14
	13		
	14		
CCLK+	15	19	CTR16
S.GND	16	1	GND
S.GND	17	2	GND
S.GND	18		
S.GND	19		
S.GND	20		
	21		
AData9-	22	44	DATAL0
AData8+	23	45	DATA1
AData7-	24	48	DATAL2
AData4+	25	5	DATA5
AData3-	26	8	DATAL6
AData2+	27	9	DATA7
	28		
BData8+	29	53	DATA9

EDT Cable 016-01961-00 (15')			
Camera Signal	Camera Pin	EDT pin	EDT signal
BDATA7-	30	56	DATAL10
BDATA6+	31	57	DATA11
BDATA5-	32	12	DATAL12
BDATA2+	33	17	DATA15
	34		
	35		
CCLK-	36	59	CTRL16
DVAL+	37	22	CTR18
IMVAL+	38	21	CTR17
	39		
	40		
	41		
	42		
ADATA8-	43	46	DATAL1
ADATA6+	44	49	DATA3
ADATA6-	45	50	DATAL3
ADATA4-	46	6	DATAL5
ADATA2-	47	10	DATAL7
	48		
	49		
BDATA8-	50	54	DATAL9
BDATA6-	51	58	DATAL11
BDATA4+	52	13	DATA13
BDATA4-	53	14	DATAL13
BDATA2-	54	18	DATAL15
	55		
	56		
S.GND	57		
DVAL-	58	62	CTRL18
IMVAL-	59	61	CTRL17
	60		

EDT Cable 016-01961-00 (15')			
Camera Signal	Camera Pin	EDT pin	EDT signal
	61		
	62		

Table 3. USPS 2-Channel Grayscale Pinout

Frame Valid Interrupts

A Frame Valid interrupt is provided to indicate to the software when an image is complete, as each image may have a different number of rasters. There is no need to flush the FIFOs between images, because only the first few words of the final status raster are required by the application.

The interrupt service routine can determine the number of rasters in the frame last acquired by reading the Vertical Last Count register.

Status Raster

When the image is complete, a final raster of status information is added to the end.

The format of this raster is as follows:

Word 0, bits 15-0	number of pixel clocks per raster as programmed into Horizontal Active registers
Word 0, bits 31-16	number of rasters captured in this image
Word 1, bits 15-0	number of raster under-runs encountered in this image
Word 1, bits 31-16	number of raster over-runs encountered in this image
Word 2, bits 15-0	number of line valid rising edges encountered since start-of-frame was detected
Word 2, bits 31-16	number of frame valid rising edges encountered since start-of-frame was detected
Word 3, bits 15-0	number of frames grabbed since reset
Word 3, bits 31-16	undefined

All remaining words in the status raster are undefined.

Registers

Table 1 lists the PCI DV FCI registers implemented with the Base Configuration firmware.

Register	Address(es)	Size (in bits)	Read/Write
Command	0x00	8	write-only
Firmware ID	0x00	8	read-only
Status	0x01	8	read-only
Configuration	0x02	8	read-write
Data Path	0x06	8	read-write
Serial Data Status	0x0B	8	read-only
Serial Data Control	0x0C	8	read-write
Utility2	0x10	8	read-write
Horizontal Active Lo	0x1A	8	read-write
Horizontal Active Hi	0x1B	8	read-write
Vertical Last Count Lo	0x1C	8	read-only
Vertical Last Count Hi	0x1D	8	read-only
Vertical Active Lo	0x1E	8	read-write
Vertical Active Hi	0x1F	8	read-write
FCI Data Path	0x28	8	read-write
USPS Control	0x29	8	read-write

Table 4. USPS Registers

Device Control Registers

Command Register

Size	8-bit
I/O	write-only
Address	0x00
Comments	Bits written to this register are strobe bits and need not be cleared after setting. When read, this register is the Firmware ID register, described next.

Bit	Name	Description
7-5	not used	
4	CLRFVINT	Setting this bit clears the frame valid interrupt.
3	CLEAR_CONT	Strobe this bit to clear the CONTINUOUS bit of the Data Path register the next time that the ACQUIRE_IP bit in the Status register is true. If ACQUIRE_IP is true when this bit is strobed, CONTINUOUS is cleared immediately.
2	not used	
1	ENABLE_GRAB	Enable acquisition of the next complete frame. If enabled in the configuration register, the shutter time is started. If the continuous acquisition bit is set in the data path register, then ENABLE_GRAB starts acquisition, which continues until the continuous bit is reset.
0	RESET_INTFC	Setting this bit resets the PCI DV camera interface circuit.

Firmware ID Register

Size	8-bit
I/O	read-only
Address	0x00
Comments	Xilinx revision, frozen at 0x02

Bit	Name	Description
7-4	not used	
3-0	REV	The Xilinx firmware revision level.

Status Register

Size	8-bit
I/O	read-only
Address	0x01
Comments	The executable watchstat (included with the PCI DV software) reads and displays this register symbolically.

Bit	Name	Description
7	AQUIRE_IP	When set, the camera interface has detected a valid beginning of frame and is presently acquiring data.
6	GRAB_ARMED	When set, the grab command has been issued and the camera interface is waiting for a valid beginning of a frame.
5-2	not used	
1	FRAME_VALID	When set, valid data is being transmitted (though the PCI DV FCI is not necessarily acquiring data).
0	OVERRUN	When set, indicates that data was lost during a frame transfer because the host was not ready to receive at the rate at which the camera was transmitting, therefore the data has been corrupted.

Configuration Register

Size	8-bit
I/O	read-write
Address	0x02

Bit	Name	Description
7-4	not used	
3	FIFO_RESET	Set and clear this bit to reset the PCI DV input FIFO.
2-0	not used	

Data Path Register

Size	8-bit
I/O	read-write
Address	0x06

Bit	Name	Description
7-5	not used	
4	CONTINUOUS	Set if PCI DV is to acquire successive frames of data. ENABLE_GRAB in the Command register must be set to start acquisition. After CONTINUOUS has been cleared, acquisition continues until the end of a complete frame. Clear in either of two ways: write 0 to this bit to clear it immediately, or strobe the CLEAR_CONT bit of the Command register to clear this bit after the next DMA transfer completes.
3	INVERT_DATA	Inverts the incoming data.
2-0	not used	

Serial Data Status Register

Size	8-bit
I/O	read-only
Address	0x0B

Bit	Name	Description
7	INTFC_INT	INTFC_INT is true when FVINT is true. INTFC_INT is ANDed with the EN_GLOB_INT bit of the serial data control register and the result passed on to the PCI Xilinx. If the RMT_EN_INTR and PCI_EN_INTR bits of the PCI interrupt and remote Xilinx configuration register in the PCI Xilinx are set (described in the PCIDV user's guide), then an interrupt is asserted over the PCI bus to the host computer.
6	FVINTSTAT	Set when a falling edge frame valid has been detected, cleared by CLR FVINT.
5	not used	

4	FVINT	Set when frame valid interrupt is enabled in through the ENFVINT bit of the Utility2 register, and FVINTSTAT is true. Clear this interrupt using the CLRFVINT in the command register.
3-0	Not used	

Serial Data Control Register

Size	8-bit
I/O	read-write
Address	0x0C

Bit	Name	Description
7-5	not used	
4	EN_GLOB_INT	Global interrupt enable. Enables all interrupts.
3-0	not used	

Utility2 Register

Size	8-bit
I/O	read-write
Address	0x10

Bit	Name	Description
7-4	not used	
3	ENFVINT	Setting this bit enables the frame-valid interrupt, which occurs on the falling edge of frame valid. Clear this interrupt with the CLRFVINT (Command register, bit 4).
2-0	not used	

Horizontal Active Lo and Horizontal Active Hi Registers

Size 8-bit

I/O read-write

Address 0x1A and 0x1B

Comments Load these registers with a 16-bit integer specifying the number of pixel clocks per raster minus 1 to be captured.

Bit	Name	Description
7-0	HACT[7-0]	Horizontal Active LSBs.

Bit	Name	Description
7-0	HACT[15-8]	Horizontal Active MSBs.

Vertical Last Count Lo and Vertical Last Count Hi Registers

Size 8-bit

I/O read-only

Address 0x1C and 0x1D

Comments A 16-bit integer specifying the number of rasters in the most recently completed frame.

Bit	Name	Description
7-0	VLCNT[7-0]	Vertical Last Count LSBs.

Bit	Name	Description
7-0	VLCNT[15-8]	Vertical Last Count MSBs.

Vertical Active Lo and Vertical Active Hi Registers

Size	8-bit
I/O	read-write
Address	0x1E and 0x1F
Comments	A 16-bit integer specifying the maximum number of rasters to accept before assuming a jam and aborting the grab. Typically set to 20,000.

Bit	Name	Description
7-0	VACT[7-0]	Vertical Active LSBs.

Bit	Name	Description
7-0	VACT[15-8]	Vertical Active MSBs.

FCI Data Path Register

Size	8-bit
I/O	read-write
Address	0x28
Comments	At power up, this register will contain 0. When this register is loaded with 0x00, the CAMERA_MODE bits of the USPS Control register determine the camera mode. If set to anything other than 0, this register determines the camera mode.

Bit	Name	Description
2-0	NUMCHAN[3-0]	Number of data channels –1 1 = 2-channel camera 3 = 4-channel camera
5-3	BITS[3-0]	Number of bits per channel –1 7 = 8 bits per pixel 0 = 1 bit per pixel
6		Not used.
7	DVAL_EARLY	If set, assume DVAL is one pixel clock early.

USPS Control Register

Size 8-bit
 I/O read-write
 Address 0x29

Comments If bits two through seven are set to zero, all video and status information is transferred in little-endian mode.

The bit video_bitswap is normally used only on four-channel black and white data. Bit video_lastswap determines which pixel channel carries the last valid pixel when filling out a raster line with an underrun error.

The CAMERA_MODE bits are only used when the FCI Data Path register is set to 0. If the FCI Data Path register is set to anything other than 0, that value will determine the camera mode.

Bit	Name	Description
7	VIDEO_SHORTSWAP	Swap shorts within each 32-bit word of video data
6	VIDEO_BYTESWAP	Swap bytes within each 16-bit short of video data
5	VIDEO_BITSWAP	Swap bits within each byte of video data
4	VIDEO_LASTSWAP	Set if last pixel is in LSBs of video data from camera.
3	STATUS_SHORTSWAP	Status raster short swap
2	STATUS_BYTESWAP	Status raster byte swap
1-0	CAMERA_MODE	00 4-channel binary black and white mode 10 2-channel 8 bit grayscale mode 11 4-channel 8 bit grayscale mode

References

PCI DV Family User's Guide

EDT Part #008-00966-10

Online at www.edt.com

Siemens Dematic *Statement of Work for Flexible Camera Interface Version 0.5*