PCI GP

PCI GP DMA Board Addendum for 4-Channel Synchronous Serial Interface Using gpssd4.bit and ssd4io.bit

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Contents

Overview

The PCI GP (20, 60, ECL)—when the PCI Flash is loaded with pcdssd.bit—implements four high-speed DMA channels between an external device and the PCI Bus. This document describes modifications to the device side of the PCI GP to collect or output data from one to four channels of synchronous serial data, made by changing the configuration data loaded into a Xilinx RAM-based programmable gate array.

Use this document with the *PCI GP User's Guide*, EDT part number 008-00965.

Synchronous Serial Interface

ssd4io.bit

When loading the PCI GP user FPGA with ssd4io.bit, a synchronous serial interface channel is composed of one data bit accompanied by one clock. The data can be configured to be sampled on the rising or the falling edge of the clock and stored or accessed in the host computer memory by the PCI GP. The PCI GP is configured with four independent serial interface channels, which can be configured individually as inputs or outputs.

gpssd4.bit

When loading the PCI GP user FPGA with gpssd4.bit, a synchronous serial interface channel is composed of one to four input data bits accompanied by a clock. The data is sampled on the rising edge of the clock and stored in the host computer memory by the PCI GP and is configured with one, two, or four independent serial interface channels. Each channel can have one, two or four data bits. Ouput is not supported.

Use the SSD4 modification with one of two optional cables. The SSD4 differential cable (EDT part number 016-00566-00) provides a differential RS-422 (PCI GP-20), LVDS (PCI GP-60), or ECL (PCI GP-ECL) interface. There is no single-ended cable for the PCI GP; the correct cable is CAB-SS-68 (EDT part number 016-01362-00). Each cable allows up to four channels: the number of active channels and data bits in each channel depends on the configuration of the PCI GP board and associated software.

Software and instructions are included to test the SSD4 and cable using a similar PCI GP and a differential cable. Standard tests will test a PCI GP as far as the back-panel connector.

Installation Modifications

Install PCI GP hardware and software according to the standard installation instructions found at www.edt.com > Technical > Documentation. Follow the appropriate steps below to modify the installation.

PCI Bus Hosts Under UNIX-based Systems

Perform the installation as specified in the standard installation instructions.

1. If necessary, at the prompt, enter:
   ```
   cd /opt/EDT/pcd
   ```
2. At the prompt, enter:
   ```
   pcdrequest
   ```
3. Select the required Xilinx programming file. The pcdrequest command will print a list of options for these files. See also “Included Files” on page 8 for more information. Pcdrequest will generate a shell script named pcdload containing commands to load the user FPGA. This shell script will automatically run at boot time.

PCI Bus Hosts Under Windows NT

1. Perform the installation as specified in the standard installation instructions.
2. When installation is complete, you’ll see an icon on your desktop labeled **Pcd Setup**. Double-click this icon.
3. Select the required Xilinx programming file. A list of options for these files will be displayed. A batch file called pcdload.bat will be created with commands to load the user FPGA. This command must be run by the user before opening the board for use.

Included Files

The following files are shipped with the PCI GP:

initpcd.c	Board hardware configuration utility. Manual included as a comment.
gpssd4.cfg	Configuration file for use with gpssd4.bit.
rd4.cfg	Configuration file for use with ssd4io.bit input.
wr4.cfg	Configuration file for use with ssd4io.bit output.
wr16.c rd16.c	Simple single-channel input and output sample programs. Use "-c <channel>" to specify channel.

User Xilinx Load Files

gpssd4.bit	Xilinx firmware file that configures the board for 4-channel operation at clock speeds to 60 MHz. Each channel consists of a clock and is programmed to have 1, 2, or 4 data bits per channel. When this bitfile is loaded, all channels are inputs only.
ssd4io.bit	Xilinx firmware or file that configures the board for four channel operation at clock speeds to 60 MHz. Each channel consists of a clock and one data bit. When this bitfile is loaded, all four channels can be programmed for input or output.

Configuration and Setup

Use initpcd and gpssd4.cfg for the SSD4, and rd4.cfg (read) or wr4.cfg (write) for the SSD4IO, to load the bitfile and setup direction and control registers.

See the documentation at the beginning of the included file, initpcd.c, for more information.

The SSD4 requires two bitfiles, the PCI bitfile and the interface bitfile. These bitfiles are described by running pcdrequest or in the text file pcd_bitfiles that is shipped with your PCD driver.

Programming the SSD4 can be accomplished using configuration files with the initpcd program, or with traditional C code. Initpcd uses ASCII configuration files to simplify and automate register configuration. Source to inipcd, initpcd.c and initedt.c are provided as sample C code for those wanting to program the registers directly.

Testing

Refer to “Verifying the Installation” in the *PCI GP User’s Manual*, EDT document number 008-00965-06.

Input and Output

Refer to the Input and Output section of the *PCI GP User's Guide.*

Example Program

ssd4io.bit

Input:

```
initpcd-f rd4.cfg
rd16 –c 2
```

Output:

```
initpcd-f wr4.cfg
wr16 –c 1
```

gpssd4.bit

```
initpcd-f gpssd4.cfg
rd16 –c 3
```

Data Formats

The GPSSD4 and SSD4IO can store data in memory from up to four different channels. GPSSD4 can have 1, 2 or 4 data bits, andSSD4IO only has one data bit. The data can be stored either least significant bit first or most significant bit first.

All four channels are always supported. The number of bits per channel and the bit storage order is determined by D0, D1, and D2 in the Funct Register. See “Funct Register” on page 21 for more information.

The following six figures illustrate the way data is stored using all valid combinations of the three bits, for the case of the single-channel configuration.

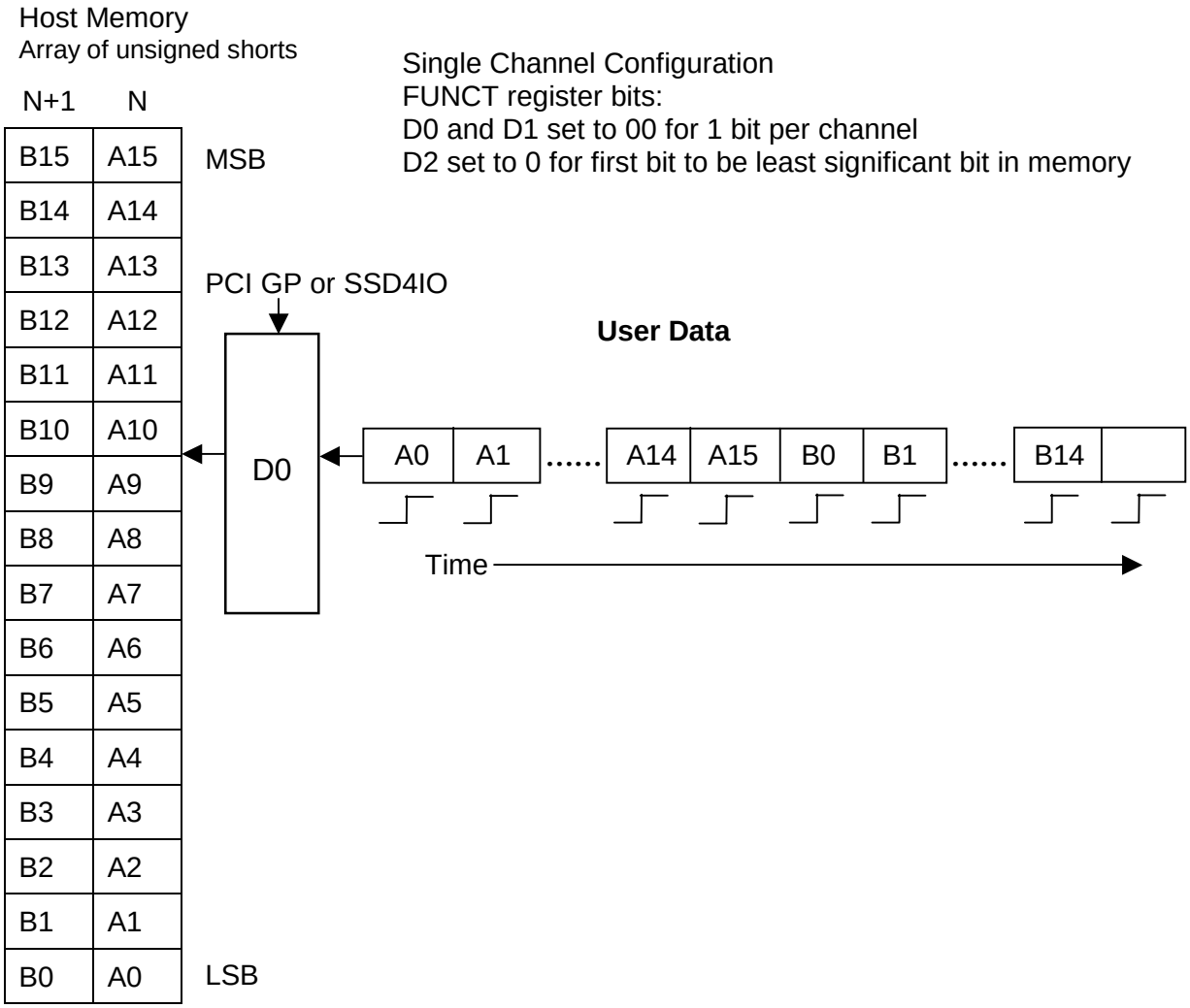

Figure 1. Single Channel, Single Bit, Least Significant Bit First

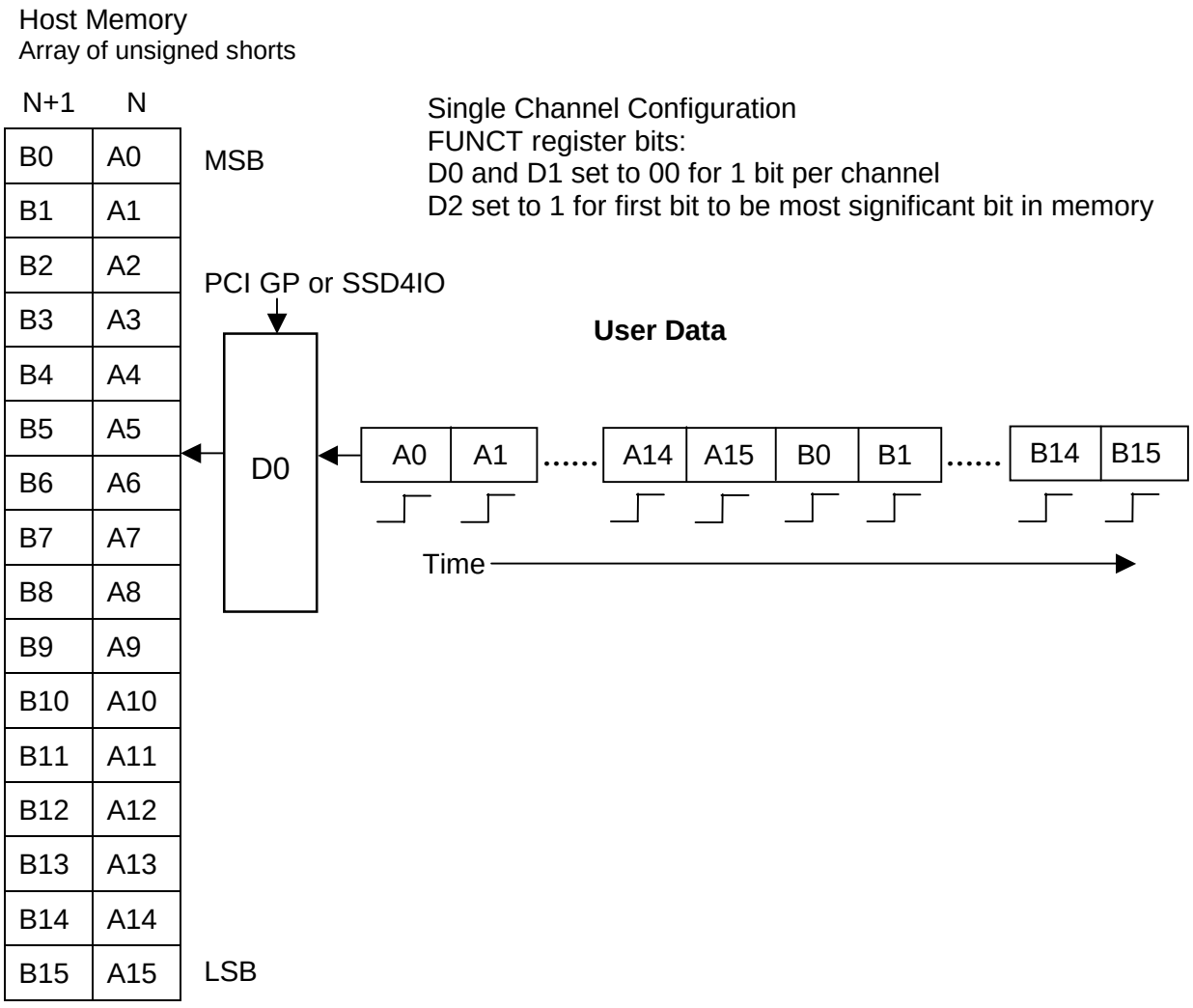

Figure 2. Single Channel, Single Bit, Most Significant Bit First

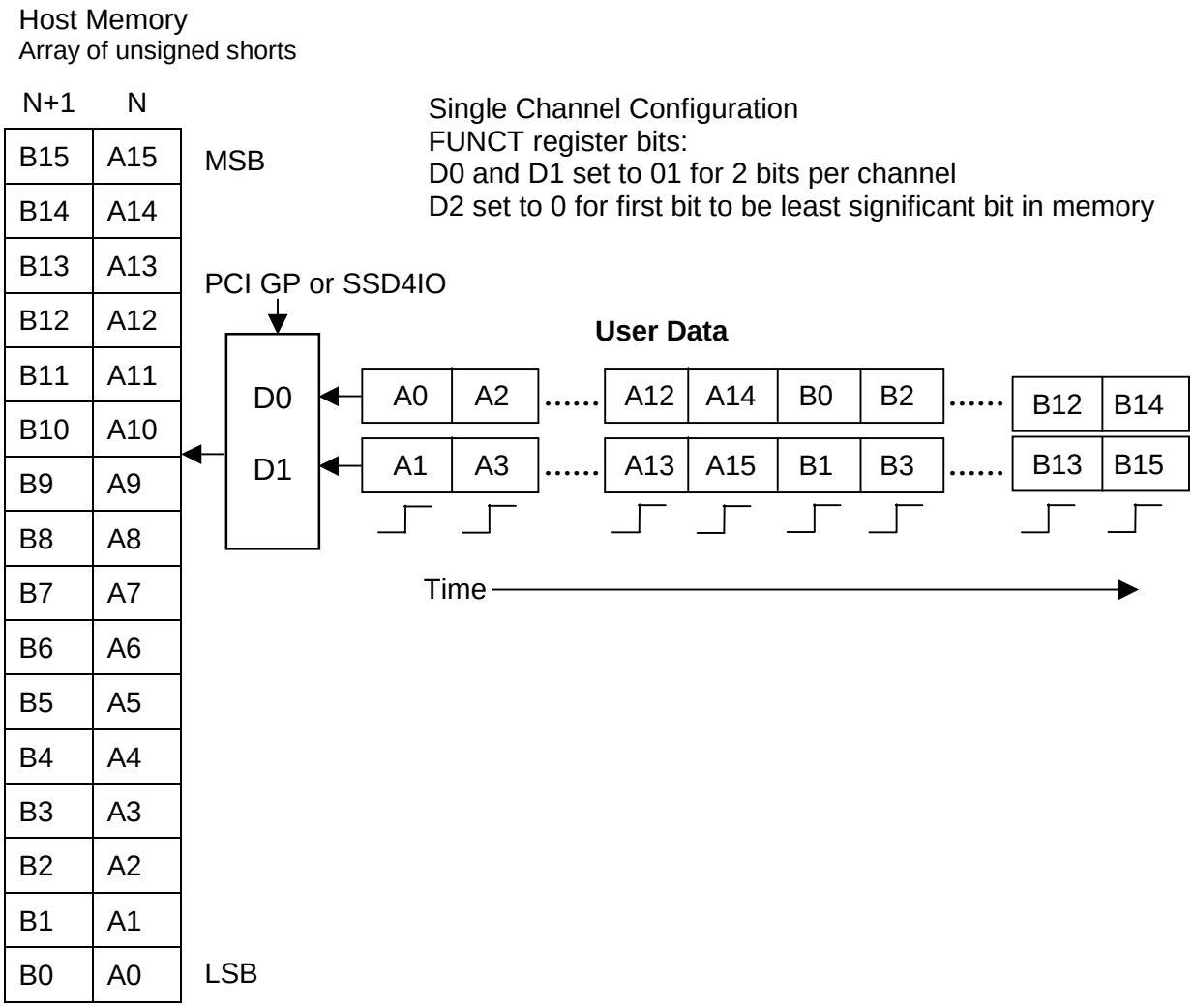

Figure 3. Single Channel, Two Bit, Least Significant Bit First

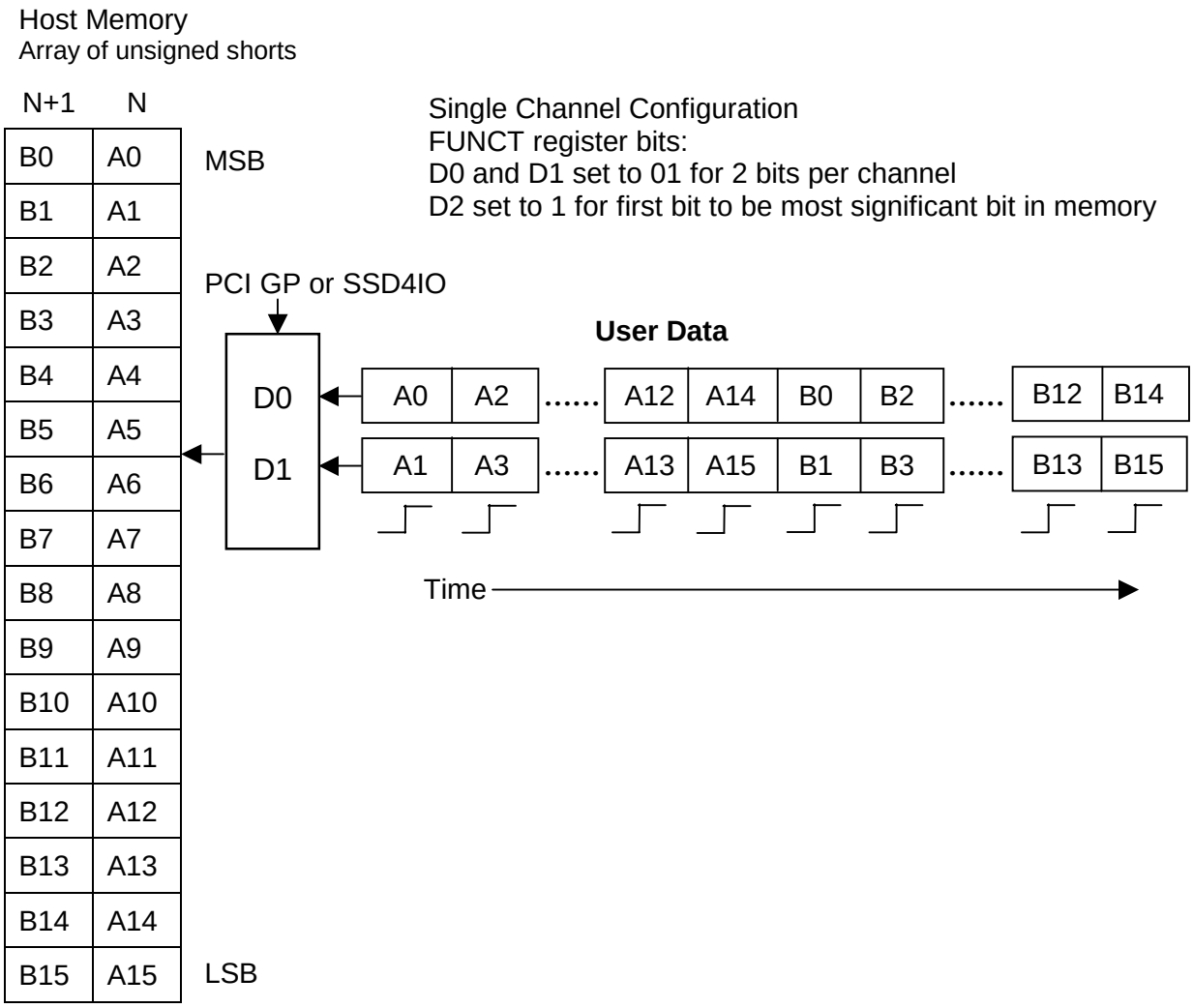

Figure 4. Single Channel, Two Bit, Most Significant Bit First

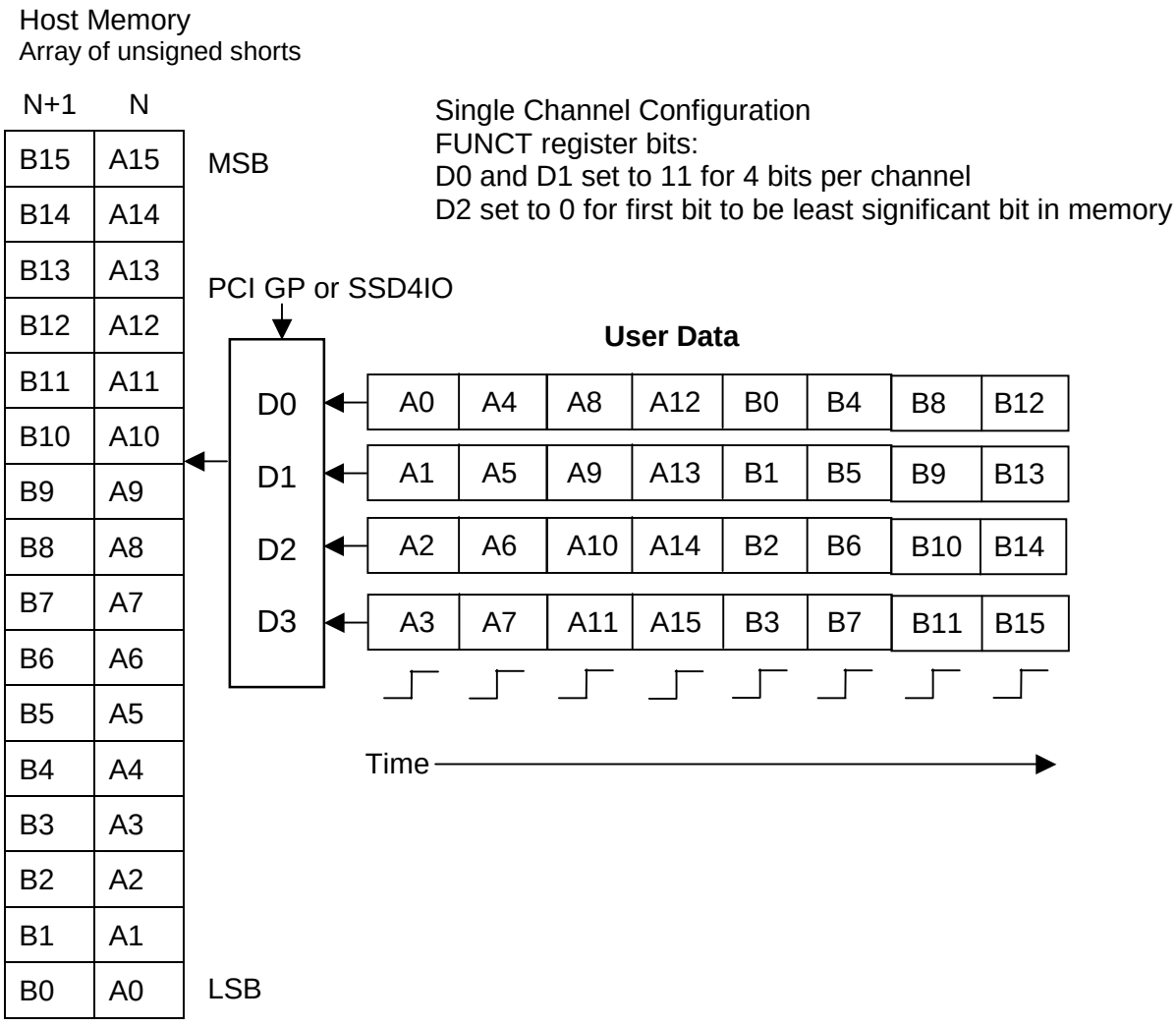

Figure 5. Single Channel, Four Bit, Least Significant Bit First

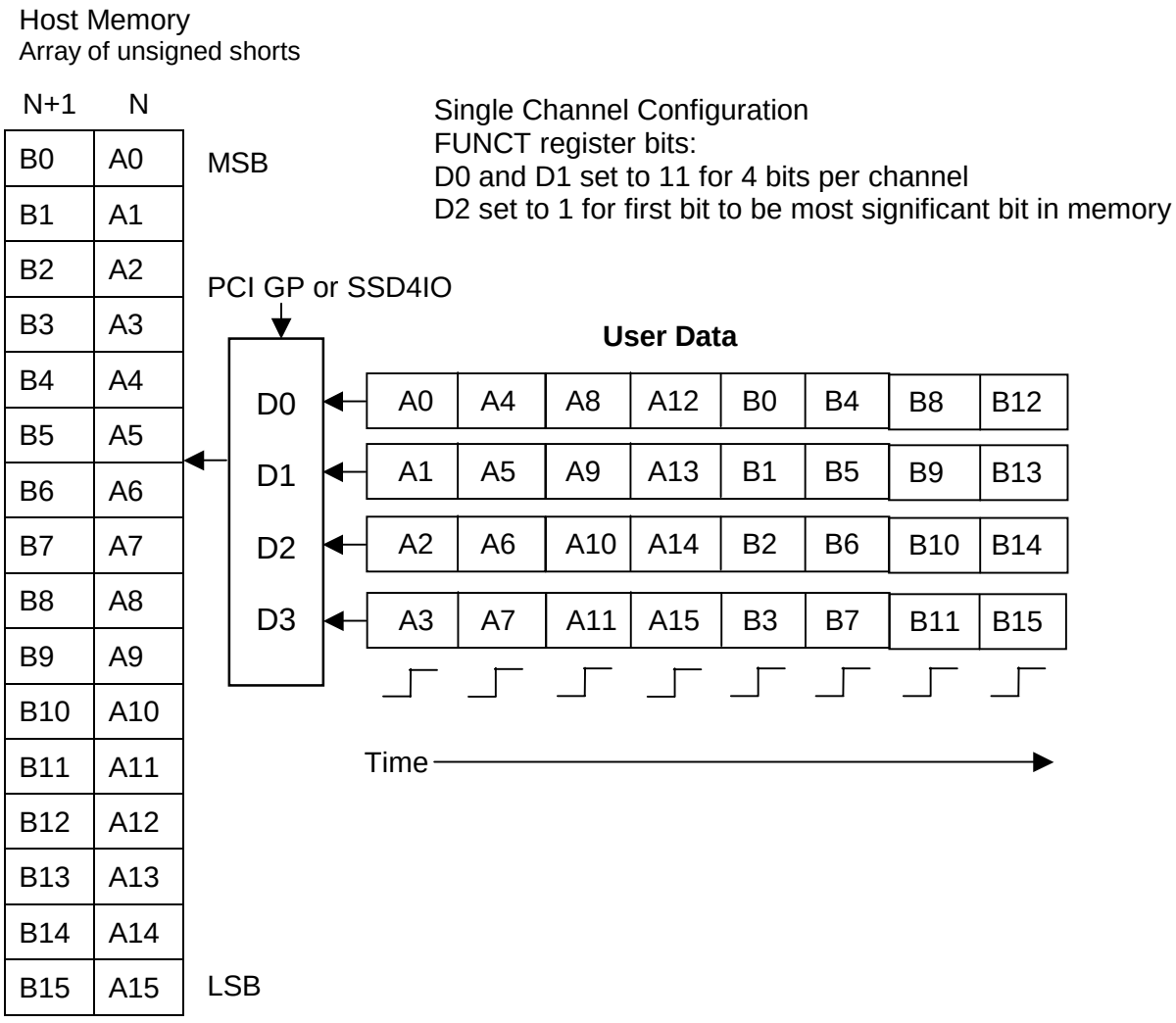

Figure 6. Single Channel, Four Bit, Most Significant Bit First

Channel Interface and Connector

When configured with GPSSD4 user Xilinx programming file, the PCI GP uses a differential cable. Each cable has one connector to attach to the PCI GP, and four 25-pin D connectors to attach to the user signals. Each of the 25-pin connectors represents inputs associated with one channel. Because the board itself has RS-422 or LVDS inputs terminated in 100 Ω, the differential cable is wired directly to the appropriate PCI GP inputs.

25-pin Connector Pinout

Pin	Differential	Pin	Differential
1	CHCLK+	14	Not connected
2	CHCLK–	15	Not connected
3	CHD0+	16	Not connected
4	CHD0–	17	Not connected
5	CHD1+	18	Not connected
6	CHD1–	19	Not connected
7	CHD2+	20	Not connected
8	CHD2–	21	Not connected
9	CHD3+	22	Not connected
10	CHD3–	23	Not connected
11	Not connected	24	Not connected
12	Not connected	25	Ground
13	Not connected		

Table 1. PCI GP 25-pin connector pinout

PCI GP Connector Pinout

AMP	Signal	AMP	Signal
1	Reserved	35	Reserved
2	CH1D0+	36	CH1D0–
3	CH1D1+	37	CH1D1–
4	CH1D2+	38	CH1D2–
5	CH1D3+	39	CH1D3–
6	CH2D0+	40	CH2D0–
7	CH2D1+	41	CH2D1–
8	CH2D2+	42	CH2D2–
9	CH2D3+	43	CH2D3–
10	CH3D0+	44	CH3D0–
11	CH3D1+	45	CH3D1–
12	Reserved	46	Reserved
13	CH3D2+	47	CH3D2–
14	CH3D3+	48	CH3D3–
15	CH4D0+	49	CH4D0–
16	CH4D1+	50	CH4D1–
17	Reserved	51	Reserved
18	Reserved	52	Reserved
19	CH4D2+	53	CH4D2–
20	CH4D3+	54	CH4D3–
21	Reserved	55	Reserved
22	Reserved	56	Reserved
23	CH2CLK+	57	CH2CLK–
24	CH3CLK+	58	CH3CLK–
25	Reserved	59	Reserved
26	Reserved	60	Reserved
27	Reserved	61	Reserved
28	Reserved	62	Reserved
29	CH1CLK+	63	CH1CLK–
30	CH4CLK+	64	CH4CLK–
31	Reserved	65	Reserved
32	Reserved	66	Reserved
33	Reserved	67	Reserved
34	Ground	68	Ground

Table 2. PCI GP pinout using gpssd4.bit

AMP	Signal	AMP	Signal
1	Not used	35	Not used
2	CH0D+	36	CH0D–
3	CH0CLK+	37	CH0CLK–
4	Not used	38	Not used
5	Not used	39	Not used
6	Not used	40	Not used
7	Not used	41	Not used
8	Not used	42	Not used
9	Not used	43	Not used
10	CH1D+	44	CH1D–
11	CH1CLK+	45	CH1CLK–
12	Not used	46	Not used
13	Not used	47	Not used
14	Not used	48	Not used
15	Not used	49	Not used
16	Not used	50	Not used
17	Not used	51	Not used
18	Not used	52	Not used
19	Not used	53	Not used
20	Not used	54	Not used
21	Not used	55	Not used
22	Not used	56	Not used
23	Not used	57	Not used
24	Not used	58	Not used
25	Not used	59	Not used
26	CH2CLK+	60	CH2CLK–
27	Not used	61	Not used
28	Not used	62	Not used
29	CH2D+	63	CH2D–
30	Not used	64	Not used
31	CH3D+	65	CH3D–
32	CH3CLK+	66	CH3CLK–
33	Not used	67	Not used
34	Ground	68	Ground

Table 7. PCI GP pinout using ssd4io.bit

Programmable Gate Array Register Modifications

After the modified Xilinx firmware files are installed, the PCI GP registers are modified as follows from those described in the *PCI GP User's Guide,* EDT part number 008-00965-06.

SSD4IO

The SSD4IO adds seven new registers (see edtreg.h): SSD16_CHENL, SSD16_CHDIRL, SSD16_CHEDGEL, SSD16_CHBITORDER, SSD16_CHUNDERFLOW, SSD16_CHOVERFLOW, and SSD4IO_TIMESTAMP.

These definitions are used in edt_intfc_read and edt_intfc_write, which are in turn used in initpcd.c for the PCD boards. Each register is eight bits wide, and each pair represents 16 bits. In the following descriptions the least significant bit configures channel 0 and the most significant bit configures channel 15.

Command Register

Size 8 bit

Address 0x00

Comments The ENABLE bit (D3) is used same as the PCI CD.

Bit	Name	Description
D0	DIR	Not used
D2	DATA_INV	Not used

Data Path Status Register

Size 8 bit

Address 0x01

Comments This register is not used.

Funct Register

Size 8 bit

I/O read-write

Address 0x02

Access PCD_FUNCT

Bit	Name	Description
D0-3	Not used	

Stat Register

Size 8 bit

Address 0x03

Comments This register is not used.

Stat Polarity Register

Size 8 bit

Address 0x04

Comments This register is not used.

Direction Control Registers

Size 8 bit

Address 0x06, 0x07

Comments These registers are not used. See Channel Direction registers.

Channel Enable Register

Size	16 bit
I/O	read-write
Address	0x10
Access	SSD16_CHEN
Comments	Used to enable each of the 16 channels. Least significant bit corresponds to channel 0. A 1 bit enables and a 0 bit disables the channel. Only four least significant bits apply to SSD4IO.

Bit	Description
D0	Enable for channel 0.
D1	Enable for channel 1.
D2	Enable for channel 2.
D3	Enable for channel 3.

Channel Direction Register

Size	16 bit
I/O	read-write
Address	0x12
Access	SSD16_CHDIR
Comments	Used to set the direction of each of the 16 channels. A 1 bit configures a channel for output, and a 0 bit configures it for input. Only four least significant bits apply to SSD4IO.

Bit	Description
D0	Direction for channel 0.
D1	Direction for channel 1.
D2	Direction for channel 2.
D3	Direction for channel 3.

Channel Clock Edge Register

Size	16 bit
I/O	read-write
Address	0x14
Access	SSD_CHEDGE
Comments	Used to configure which clock edge each channel will use to latch data. A 1 bit latches data on the rising clock edge, while a 0 bit latches data on the falling edge. Only four least significant bits apply to SSD4IO.

Bit	Description
D0	Clock edge for channel 0.
D1	Clock edge for channel 1.
D2	Clock edge for channel 2.
D3	Clock edge for channel 3.

Channel Bit Order Register

Size	16 bit
I/O	read-write
Address	0x16
Access	SSD16_CHBITORDER
Comments	Used to configure the data bit order. A 1 bit makes the LSB first; a 0 bit makes the MSB first. Only four least significant bits apply to SSD4IO.

Bit	Description
D0	Bit order for channel 0.
D1	Bit order for channel 1.
D2	Bit order for channel 2.
D3	Bit order for channel 3.

Channel Underflow Detection Register

Size	16 bit
I/O	read-only
Address	0x18
Access	SSD16_CHUNDERFLOW
Comments	Latches to a 1 if underflow is detected. To clear all the underflow bits, clear the enable bit in the Command Register. Only four least significant bits apply to SSD4IO.

Bit	Description
D0	Underflow bit for channel 0.
D1	Underflow bit for channel 1.
D2	Underflow bit for channel 2.
D3	Underflow bit for channel 3.

Channel Overflow Detection Register

Size	16 bit
I/O	read-only
Address	0x1A
Access	SSD16_CHOVERFLOW
Comments	Latches to a 1 if overflow is detected. To clear all the overflow bits, clear the enable bit in the Command Register. Only four least significant bits apply to SSD4IO.

Bit	Description
D0	Overflow bit for channel 0.
D1	Overflow bit for channel 1.
D2	Overflow bit for channel 2.
D3	Overflow bit for channel 3.

Time Stamp Register

Size	8 bit
I/O	read-write
Address	0x20
Access	SSD4IO_TIMESTAMP
Comments	Time stamp data for channel 0 are input to channel 2, and time stamp data for channel 1 are input to channel 3. The time stamp signal is input to the channel 2 clock input pin. The time stamp reset signal is input to the channel 3 clock input pin.

Bit	Name	Description
0	TS0	Enable time stamp for channel 0.
1	TS1	Enable time stamp for channel 1.
2	TS2	Use input clock on channel 2 to drive output clocks for channels 0 and 1. Data output and clock on channel 0 will be replicated on channel 1.
7-3	Not used	

SSD4

The following registers apply to gpssd4.bit.

Command Register

Size	8 bit
I/O	read-write
Address	0x00
Access	PCD_CMD

Bit	Name	Description
D0-2		Not used
D3	ENABLE	Set to one to enable the PCI GP interface. This bit is set after the direction is chosen and typically after the first DMA buffer is ready. To reset direction or flags, this bit must be reset. To flush the DMA FIFOs, clear then set this bit.
D4-7		Not used

Data Path Stat Register

Size	8 bit
Address	0x01
Comments	This register is not used.

Funct Register

Size	8 bit
I/O	read-write
Address	0x02
Access	PCD_FUNCT
Comments	The FUNCT(2:0) signals are used to set the data acquisition mode. FUNCT3 is not used.

Bit	Name	Description
D0-1		Specify the number of data bits acquired on each clock as specified below. All channels are controlled together. **D1** **D0** **Data Bits Acquired** 0 0 Only bit 0 of each channel is acquired with each clock 0 1 Bits 0 and 1 of each channel are acquired with each clock. 1 0 Undefined 1 1 Bits 0 through 3 of each channel are acquired on each clock.
D2		Controls the order in which the acquired data is placed in each one-bit word stored in the host memory. If set to high, the first bit acquired is placed in the most significant bit of the 16-bit word. If set to low, the first bit acquired is placed in the least significant bit of the 16-bit word. If multiple data bits are acquired per clock, the most significant data bit is considered the first bit.
D3-7		Not used

Data Path Stat Register

Size	8 bit
Address	0x03
Comments	This register is not used.

Polarity Register

Size	8 bit
Address	0x04
Comments	This register is not used.

Interface Configuration Register

Size	8 bit
I/O	read-write
Address	0x0F
Access	PCD_CONFIG

Bit	Name	Description
D0	BYTESWAP	Set to one to swap the order of bytes ina 16-bit word of data coming in from the camera.
D1-2		Not used
D3	SHORTSWAP	Set to one if the host computer writes the first 16-bit word on bits 16-31 of the PCI data bus (big-endian format) instead of bits 0-15 as defined in the PCI bus specification.
D4-7		Not used