RFx Gain Control

Table of Contents

Analog AGC (AAGC)

The analog gain path can be manually controlled by disabling the AGC and writing the desired gain to the initial gain setting (AgcInitGain_dB).

The Analog Automatic Gain Control block (AAGC) measures the average power of the digitized input signal and issues gain adjustments to a digital step attenuator (DSA) and two variable gain amplifiers (VGA) preceding the analog to digital converter (ADC) in order to maintain proper amplitude loading at the ADC. By maintaining proper ADC loading, the dynamic range of the input signal is maximized. Figure 1 and Figure 2 illustrate the feedback path of the VGA, ADC, and AAGC (only a single VGA is shown for simplicity, but the AGC actually controls the DSA and two VGAs in the input path). The DSA has four selectable attenuation values: 0, 6, 12, and 18 dB. One VGA has a range of 0 to 40 dB in 0.5 dB steps, and one VGA has two settings: 0 and 10 dB. Due to the coarse steps in attenuation and gain (in one of the VGAs), values are distributed among the components in order to minimize large gain jumps.

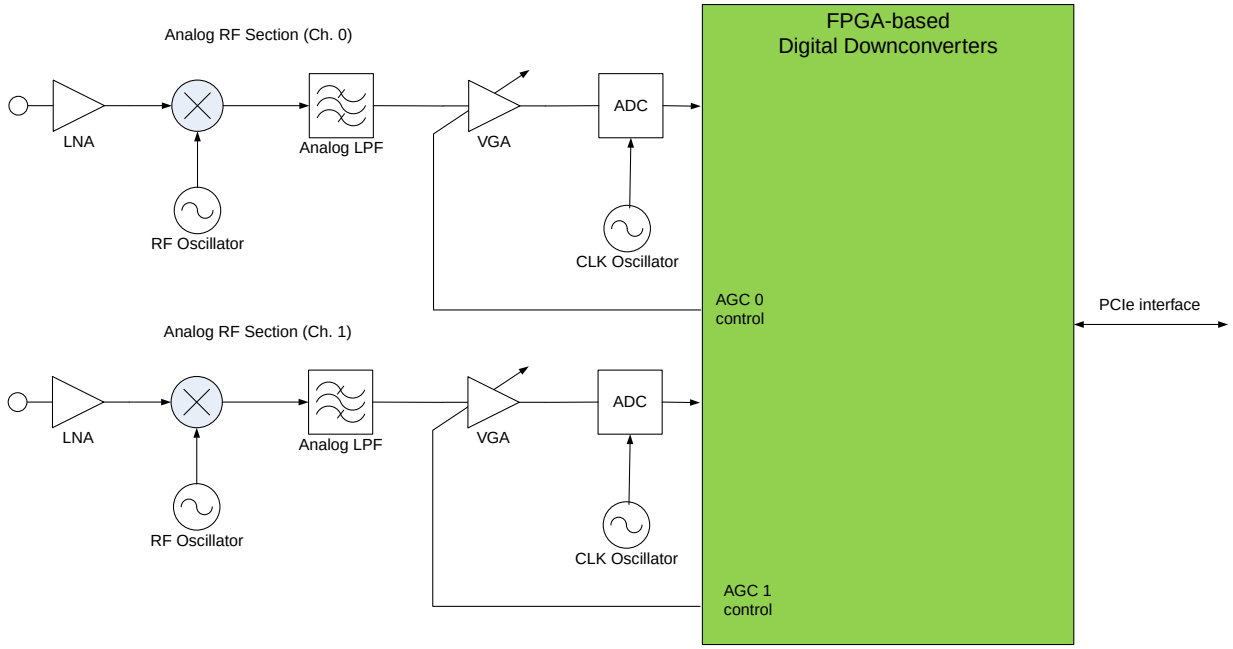

Figure 1. Simplified digital radio block diagram

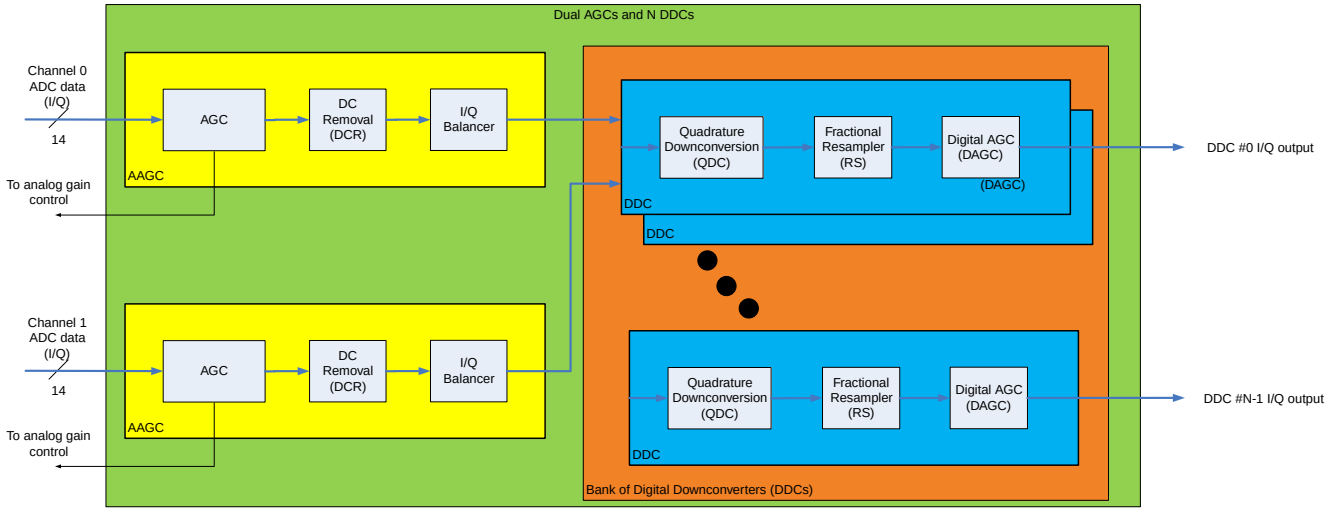

Figure 2. Major processing blocks in Dual AGC and DDC design

The AAGC block also contains a DC removal function and an I/Q balancer function. The DC removal function estimates the DC content of the input signal and subtracts it out. The I/Q balancer function adaptively estimates the phase and gain imbalances in the signal and compensates accordingly in order to minimize any unbalances. A DC offset and some I/Q imbalance are typical in zero IF (intermediate frequency) downconversion receivers.

The AAGC's behavior is controlled by several parameters. The relationship between these timing and level parameters is illustrated in Figure 3. The AAGC tries to maintain a constant average input power level to the ADC by adjusting the analog gain settings. The power level maintained is determined by the value of AgcBackoff_dB, which is the power level below full scale ADC input that is desired. When a signal is present, the AAGC increases (or decreases) the gain to the analog components based on the "attack" time constant, AgcAttackSeconds.

The smaller this time constant is, the more slowly the AAGC adjusts the gain until the steady-state value is achieved. If the signal fades (drops out) below a loss of signal (AgcLos) power threshold (AgcLosPowerThresh_dB) after a lock status (AgcLock) has been achieved, the AAGC's behavior is controlled by the AgcLosMode setting. If in ***decay*** mode, the gain decays back down (or up) to the initial gain setting (AgcInitGain_dB) based on the "decay" time constant, AgcDecaySeconds. If in ***hold*** mode, the AAGC holds its current gain value. To exits a LOS condition, the average input signal power must reach or exceed the return of signal (ROS) power threshold (AgcRosPowerThresh_dB).

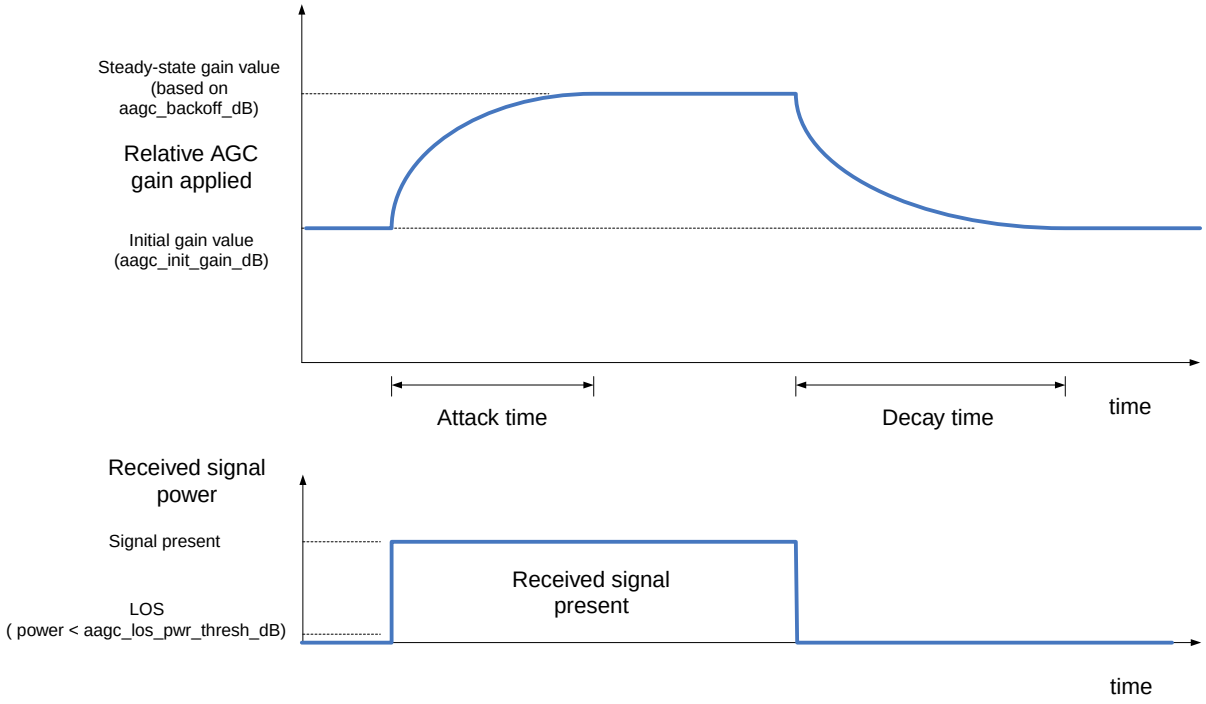

Figure 3. Relationship between signal level and attack and decay parameters for AAGC

Because the AAGC can only measure the power of the signal after the ADC, problems can occur if the initial gain is set too low or too high. If the initial gain is set too low (when AgcLosMode is in decay mode) and a signal dropout occurs, the AAGC will drive the gain to the initial gain setting. Once the signal level returns (at the input to the analog components), the measured signal power may not be above the ROS power threshold setting thus causing the AAGC to remain in an LOS condition. A diagram depicting the level parameters relative to one another is shown in Figure 4. A similar problem can occur if the initial gain setting (AgcInitGain_dB) is set too high which can overdrive the ADC causing it to clip or saturate its output levels. Major nonlinear distortion occurs when the ADC is driven into saturation and can actually cause the AAGC's average power measurements to appear as if they are low or even an LOS condition is occurring. One way to detect this condition is to read the AgcClip indicator to see if the clip count is changing. If so, resetting the AAGC and lowering the initial gain setting (AgcInitGain_dB) and/or increasing the AgcBackoff_dB value should alleviate the situation and allow the AAGC to lock.

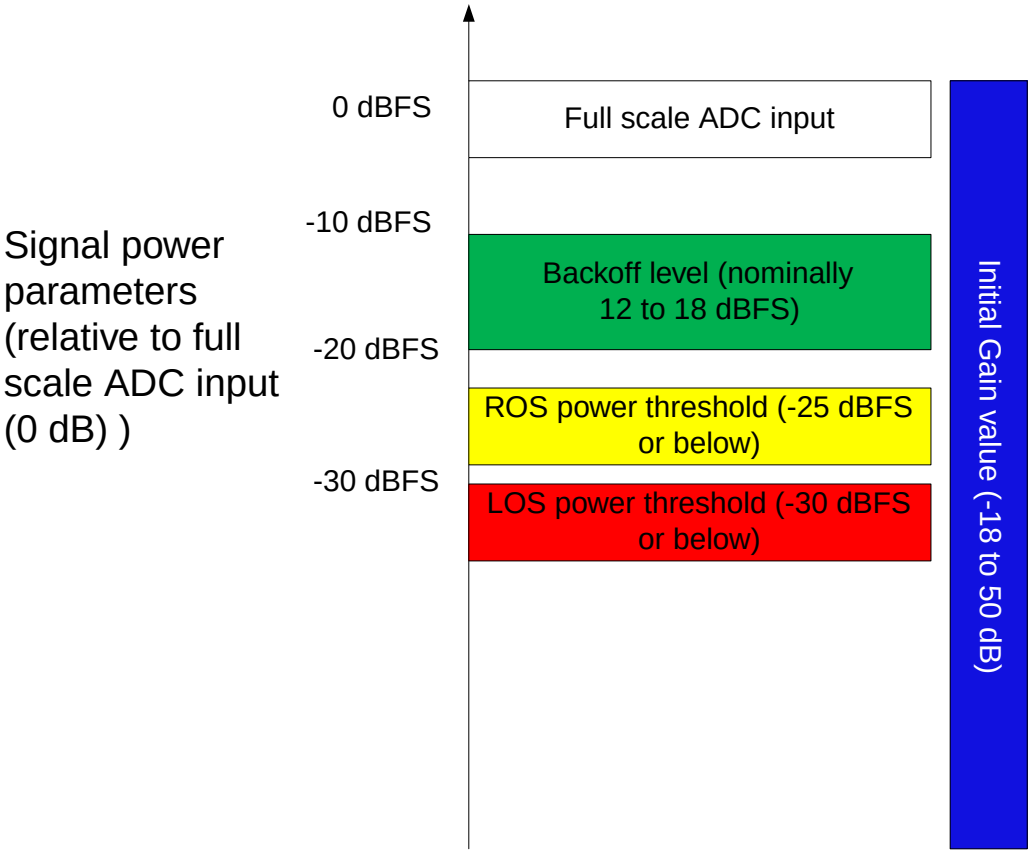

Figure 4. Relative signal level parameters

In most cases, a low initial gain setting is optimal in order to avoid clipping effects. Then the only situation that can potentially cause problems is the LOS situation described above.

Settings

Name	Description	Range
IQBalanceEnable	Enables I/Q balancing function. Estimates and removes phase and gain imbalances from input signal. 0 = Disable 1 = Enable	0 or 1
IQBalanceAdaptationRate	IQ Balancing adaptation rate. Larger rate values allow the function to converge faster, but with less precision (greater variance). Smaller values converge more slowly, but with less variance. 0 = 2^-13 1 = 2^-14 2 = 2^-15 3 = 2^-16	0 - 3

Name	Description	Range
DCRemovalEnable	Enables DC removal function. Estimates and removes DC content of input signal. DC is removed prior to IQ balancing function and in general should be enabled to improve operation of IQ balancing function. 0 = Disable 1 = Enable	0 or 1
AgcInitGain_dB	Sets AAGC initial gain value (in dB). The initial gain value is used as the starting value for the AAGC acquisition and tracking loop and is also the value that the AAGC loop will drive toward during a loss of signal (decay mode). If the initial gain value is set too low, then after a loss of signal condition, the input power may never reach the ROS power threshold. When the AAGC is disabled (manual mode), the initial gain value is used to set the gain manually.	-18 to 50
AgcBackoff_dB	Sets AAGC power backoff (in dBFS) from full scale ADC input power (0 dB reference). A 0 value would maintain a full scale input to the ADC. Positive values will decrease the power of the signal at the ADC's input to avoid saturating the ADC's input (clipping), typical applications might require 2-bits of headroom between peak and average amplitude (3 dB/bit for amplitude), which translates to 12 dB of backoff (6 dB/bit for power). The amount of backoff is dependent on the PAPR (Peak to Average Power Ratio) for the signal environment being operated in, but a backoff of at least 12 – 18 dB is recommended in most cases.	0 to 63
AgcAttackSeconds	Sets AAGC "attack" time constant that is used in the AAGC loop. The time constant, if thought of as 16-bit integer value, is divided by `2^31` in the FPGA design and used as a loop parameter. The smaller the value used, the slower the loop converges. The nominal time delay for a given constant value is `2^31 / (Fs*tc)`, giving a delay range from 1.3107e-4 to 8.5899 seconds in factors of 1.3107e-4 seconds at an ADC sample rate of 250 MHz. tsec = `2^31 / (Fs*tc)` tc = `round( 2^31 / (Fs*tsec) )`	1.3107e-4 to 8.5899

Name	Description	Range
AgcDecaySeconds	Sets AAGC “decay” time constant that is used in the AAGC loop. The time constant, if thought of as 16-bit integer value, is divided by `2^31` in the FPGA design and used as a loop parameter. The smaller the value used, the slower the loop converges. The nominal time delay for a given constant value is `2^31 / (Fs*tc)`, giving a delay range from 1.3107e-4 to 8.5899 seconds in factors of 1.3107e-4 seconds at an ADC sample rate of 250 MHz. tsec = `2^31 / (Fs*tc)` tc = `round( 2^31 / (Fs*tsec) )`	1.3107e-4 to 8.5899
AgcLosPowerThresh_dB	Sets AGC LOS (loss of signal) power threshold. The LOS power threshold is the value (in linear units) below full scale power (1.0) that is considered a loss of signal. An LOS condition is declared if the average input power drops below this threshold after the AGC locks. Upon detection of an LOS condition, the AGC holds its current gain value until an ROS condition occurs. The LOS power threshold should be set substantially below the power set point level (set to 1.0) so that minor variances in input signal power are not considered signal losses. Setting this value to 0 effectively disables LOS detection.	-128 to 127
AgcRosPowerThresh_dB	Sets AAGC ROS (return of signal) power threshold (in dBFS). The ROS power threshold is the value (in dB) below full scale power (0 dB) that is considered a return from a loss of signal (AgcLos) status. Once an LOS condition occurs, the AAGC behavior is controlled by the los_mode setting. Average input power must reach the ROS power threshold or above to exit the LOS state and resume normal AAGC behavior. The ROS power threshold should be set higher (less negative) than the LOS power threshold.	-128 to 127
AgcLosMode	Selects behavior of AAGC when loss of signal (AgcLos) is detected. 0 = Enters decay mode: AAGC decays to initial gain setting 1 = AAGC holds current gain setting	0 or 1
AgcLockThresh	Sets AAGC lock threshold. When the AAGC mean-squared error (AgcMse) falls below the lock threshold, the AAGC loop is declared to be locked.	0 to 3.9

Name	Description	Range
AgcUnlockThresh	Sets AAGC unlock threshold. When the AAGC mean-squared error (AgcMse) rises above the unlock threshold, the AAGC loop is declared to be unlocked.	0 to 3.9

Sensors

Name	Description	Range
AgcAvgInputPower_dBFS	AAGC average input power (relative to full scale input) in dBFS units. With the current implementation, the minimum input power that can be measured is -69.24 dBFS. (in dBFS units)	0 to -69.24
AgcGain_dB	AAGC gain value in linear units. The total gain/attenuation calculated and then applied across VGA #0, VGA #1, and the DSA.	-18 to 50
AgcClip	AAGC clip count. The clip count is a free running counter value that increments each time either the I or Q value into the AGC reaches its maximum positive or negative value. If this value is changing when read repeatedly, it may be an indication that the initial AAGC gain value (AgcInitGain_dB) is set too high and/or the AAGC power backoff (AgcBackoff_dB) is set too low (i.e. the peak to average power ratio of the input signal is large).	0 to 4095
AgcMse	AAGC mean-squared error status.	0 to 7.9
AgcLock	AAGC lock status. 0 = Unlocked 1 = Locked	0 or 1
AgcLos	AAGC loss of signal status. 0 = No LOS 1 = LOS condition	0 or 1

Initialization steps

1. Set IQBalanceEnable = 1 to minimize I/Q imbalances.
2. Set DCRemovalEnable = 1 to remove DC offset in input signal.
3. Set AgcLosMode appropriately.
4. Set AgcAttackSeconds and AgcDecaySeconds loop parameters according to the signal

environment.

5. Set AgcBackoff_dB based on peak to average power ratio of signal environment.
   Use 12-18 dB if nothing else is known about the environment.
6. Set AgcLockThresh and AgcUnlockThresh values appropriately.
   Recommended values are 0.01 and 0.5, respectively.
7. Set AgcLosPowerThresh_dB, AgcRosPowerThresh_dB, and AgcInitGain_dB parameters.
   Recommended values are -30 dB, -25 dB, and -18 dB, respectively, if loss of signal (LOS) detection is desired.
   Otherwise recommended values are -128 dB, -20 dB, and -18 dB, respectively, to disable LOS detection.

Digital AGC (DAGC)

The digital AGC block removes gain applied during the decimation process and, when the DAGC loop is enabled, normalizes the average output power to unity for follow-on processing.

The DAGC loop maintains a constant average signal level at the start of the digital signal processing (DSP) chain. This is important for linear modulation schemes like PSK and QAM, where the receiver decision regions are based on an expected average signal level.

Variations in the average signal level can lead to increased symbol errors, which the digital AGC compensates for.

Settings

Name	Description	Range
DagcEnable	Enable/disable DAGC loop.	1 or 0

DagcLoopBw	Set DAGC Ki (integral gain) and Kp (proportional gain) loop parameters according to formula for user designated bandwidth of loop.
	
	This simultaneously sets the values for both:
	
	`double dPI = 4.0 * atan(1.0);`
	`double eta = sqrt(2) / 2;`
	`double theta = 2 * dPI * dagc_loop_bandwidth;`
	
	`double ki = (4 * theta * theta) / (1 + 2 * eta * theta + theta * theta);`
	`double kp = (4 * eta * theta) / (1 + 2 * eta * theta + theta * theta);`
	
	`unsigned int pi_loop_ki = round(ki * pow(2, 24));`
	`unsigned int pi_loop_kp = round(kp * pow(2, 15));`
		Floating point.

Name	Description	Range
DagcRosPowerThresh	Sets DAGC ROS (return of signal) power threshold. The ROS power threshold is the value (in linear units) below full scale power (1.0) that is considered a return from a loss of signal (DagcLos) status. Average input power must reach the ROS power threshold or above to exit the LOS state and resume normal DAGC behavior. The ROS power threshold should be set higher than the LOS power threshold.	0 to 1.99
DagcLosPowerThresh	Sets DAGC LOS (loss of signal) power threshold. The LOS power threshold is the value (in linear units) below full scale power (1.0) that is considered a loss of signal. An LOS condition is declared if the average input power drops below this threshold after the DAGC locks. Upon detection of an LOS condition, the DAGC holds its current gain value until an ROS condition occurs. The LOS power threshold should be set substantially below the power set point level (set to 1.0) so that minor variances in input signal power are not considered signal losses. Setting this value to 0 effectively disables LOS detection.	0 to 1.99
DagcLockThresh	Sets DAGC lock threshold. When the DAGC mean-squared error (DagcMse) falls below the lock threshold, the DAGC loop is declared to be locked. Recommended value is 0.01 .	0 to 3.9
DagcUnlockThresh	Sets DAGC unlock threshold. If the DAGC MSE (DagcMse) rises above the unlock threshold, the DAGC loop is declared to be unlocked. Recommended value is 0.5 .	0 to 3.9

Sensors

Name	Description	Range
DagcLos	DAGC LOS (loss of signal) status. 0 = No LOS 1 = LOS condition	0 or 1
DagcLock	DAGC lock status. 0 = Unlocked 1 = Locked	0 or 1
DagcMse	DAGC mean-squared error status.	0 to 7.9
DagcGain_dB	DAGC gain value. Sample of time varying gain applied after compensating for natural decimator gain.	0 to 255