Engineering Design Team (EDT) - Certificate of Volatility

Model:	Part Number:	Address:
PCI GS main board (all variations & revisions)	019-02063, 019-02135	**Engineering Design Team, Inc.** 3423 NE John Olsen Avenue Hillsboro, OR 97124 U.S.A. +1-503-690-1234 or 1-800-435-4320

Volatile Memory

Does the device contain volatile memory (memory whose contents are lost when power is removed)?
☑ Yes ☐ No If yes, describe the type, size, function, and steps to clear the memory below

Type (SRAM, DRAM, etc):	Size:	User Modifiable:	Function:	Steps to clear memory:
FPGA: Xilinx XC2S200-6FG456C	5292 logic cells. 56Kbit Block RAM.	☐ Yes ☑ No	DMA logic, RAM used as FIFOs for buffering. Commonly referred to as the "PCI FPGA"	Power down
FPGA: Xilinx XC2VP50-5FF1517C or XC2VP70-5FF1517C	53,136 or 74,448 logic cells. 4,176K or 5,904K bits Block RAM.	☑ Yes ☐ No	Data processing logic and interface between mezzanine card and "PCI FPGA". Commonly referred to as the "UI FPGA".	Power down
SRAM: GSI Technology GS8160Z36BGT-150	18Mbit per SRAM IC. One or two may be installed.	☐ Yes ☑ No	Used by some "UI FPGA" designs to buffer and assist in data processing. One or two SRAM's may be installed.	Power down
DRAM: Micron MT16VDDF12864HY-40BJ1	1GByte	☐ Yes ☑ No	Optionally installed. Used by some "UI FPGA" designs to buffer and assist in data processing.	Power down

Non-Volatile Memory

Does the device contain non-volatile memory (memory whose contents are retained when power is removed)?
☑ Yes ☐ No If yes, describe the type, size, function, and steps to clear the memory below

Type (Flash, EEPROM, etc):	Size:	User Modifiable:	Function:	Steps to clear memory:
CPLD: Xilinx XC9572XL-10VQG64C	72 macrocells	☐ Yes ☑ No	Configuration control: configures the "PCI FPGA" from flash on board power up	JTAG. Contact EDT.
NOR Flash: Cypress AM29LV081B-70ED	8Mbit	☑ Yes ☐ No	Configuration memory: stores "PCI FPGA" configuration bitfiles	EDT's pciload program. Contact EDT.

Mass Storage

Does the device contain mass storage memory (Hard Disk Drive, Tape Backup)?
☐ Yes ☑ No If yes, describe the type, size, function, and steps to clear the memory below

Type (HDD, Tape, etc):	Size:	User Modifiable: ☐ Yes ☐ No	Function:	Steps to clear memory:

USB

Does the item accept USB input and if so, for what purpose (i.e. Print Jobs, device firmware updates, scan upload)?
☐ Yes ☑ No If yes, describe the type, size, function, and steps to clear the memory below

Can any data other than scan upload be sent to the USB device)?
☐ Yes ☑ No If yes, describe the type, size, function, and steps to clear the memory below

RF/RFID

Does the item use RF or RFID for receive or transmit of any data including remote diagnostics (e.g. Cellular phone, Bluetooth)?
☐ Yes ☑ No If yes, describe the type, size, function, and steps to clear the memory below

Purpose:	
Frequency:	Bandwidth:
Modulation:	Effective Radiate Power (ERP):
Specifications:	

Other Transmission Capabilities

Does the device employ any other methods of non-wired access to transmit or receive any data whatsoever (e.g. anything other than standard hard wired TCP/IP, direct USB, or parallel connections)? ☐ Yes ☑ No If yes, describe below

Frequency:	Bandwidth:
Modulation:	Effective Radiate Power (ERP):
Specifications:	

Other Capabilities

Does the device employ any other method of communications such as a Modem to transmit or receive any data whatsoever?
☑ Yes ☐ No If yes, describe below:

The PCI GS mainboard is provides a base platform for data processing and DMA capabilities over the PCI bus standard. Mezzanine cards attach to the PCI GS mainboard to provide various and different transmit and receive capabilities.

Specifications:

Author Information

Name	Title	Email	Department
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