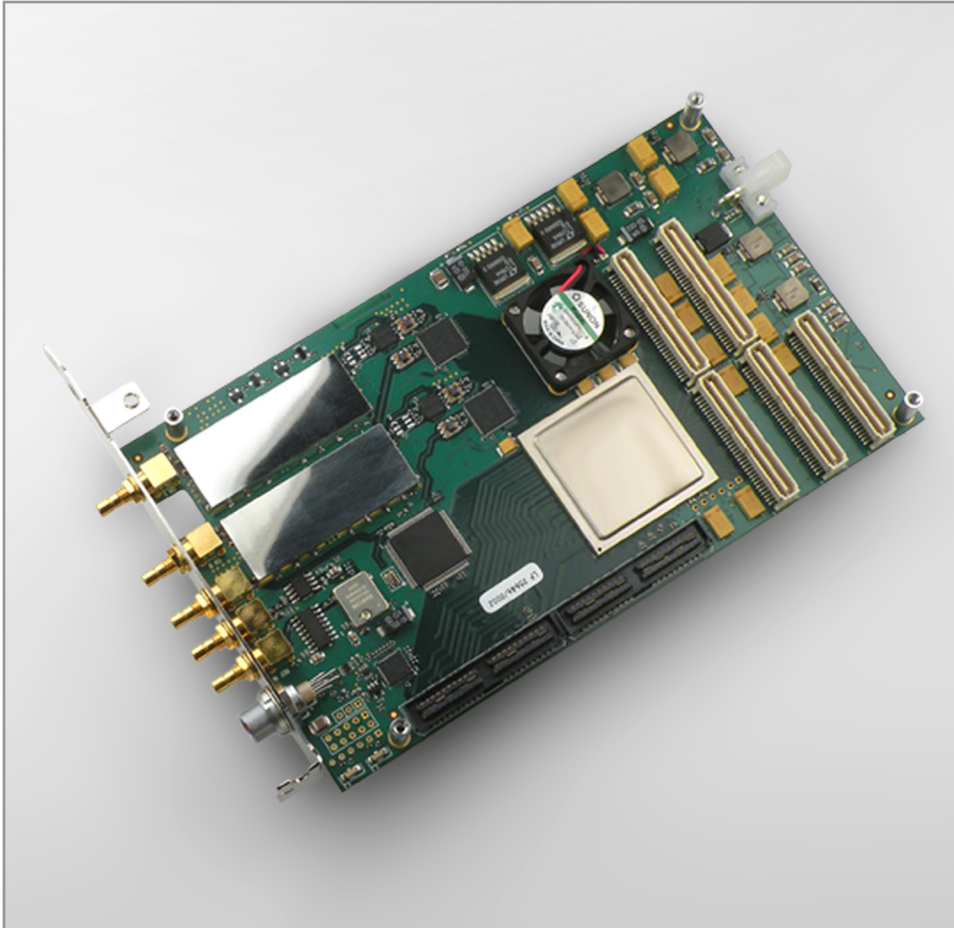


DRX16

Dual digitizer for DSP with 16-bit ADCs



Description

The DRX16 is a mezzanine board that pairs with a PCIe main board to digitize two independent IF signals, each via its own port and 16-bit ADC. EDT firmware and software are included for basic signal capture and spectral display.

Custom FPGA-based DSP designs are available for such applications as: wideband software-defined radio; real-time signal acquisition and analysis / test and measurement; adaptive signal processing; and high-speed filtering.

The board has a configurable Xilinx Virtex 6 LX FPGA (XC6VLX240T) and two identical ports for 2 to 300 MHz. The ports can be filled with two no-gain input direct modules (IDX, option A), or two fixed-gain input direct modules (IDX-FG, option B) with independent gain settings.

Output is digitized via ADCs and captured in the FPGA, which performs DSP or routes data to the main board.

Each port has a sample clock that is independently programmable from 10 to 130 MHz. A third clock is available via the sample clock I/O connector, which can be set as input or output.

The timebase can be the 10 MHz TCXO provided by EDT, or another source linked to the reference input. A reference output and a time code input (1 pps or IRIG-B) also are included.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Applications

- Wideband software-defined radio
- Test and measurement / real-time signal acquisition and analysis
- Surveillance / spectrum monitoring
- Adaptive signal processing
- High-speed filtering

Features

Mezzanine board – pairs with an EDT main board (PCIe), which adds DMA, programmable FPGA resources, and memory

Digitizes two independent IF signals via two ports with 16-bit ADCs

DSP: Custom FPGA-based design and integration services available

FPGA: One programmable Xilinx Virtex 6 (XC6VLX240T)

Ports: Two identical – each with one input direct module (IDX) for 2 to 300 MHz, with two gain options...

- Option A, two IDX modules: no gain
- Option B, two IDX-FG modules: fixed gain (it can be different on each module)

ADCs: Two 16-bit (one per port)

Sample clocks: Independently programmable for each port (10 to 130 MHz)

Sample clock I/O: Programmable as input or output

Timebase: 10 MHz TCXO or reference input, available via reference output

Time code: 1 pps or IRIG-B input

Specifications

Product Type	Dual IF digitizer for DSP with 16-bit ADCs; it requires an EDT PCIe main board.																																		
FPGA-based DSP	Custom designs available by request.																																		
FPGAs and Memory	One programmable FPGA (Xilinx Virtex 6 LX (XC6VLX240T), plus FPGA and memory resources on main board.																																		
Sample Clock	User-configurable & phase-locked to timebase	10 to 130 Msps (independently programmable for each port)																																	
ADCs (one per port)	Resolution / maximum sample rate	16 bits / 130 Msps																																	
Data Rates	Dependent on such factors as data format, main board, and system variables.																																		
Data Format (I/O)	<p>Two identical user-configurable ports, each supporting one user-configurable input direct module (IDX) One time code input from external receiver (1 pps or IRIG-B, with user-configurable output) One reference input (for user-supplied timebase, if desired) One reference output One sample clock I/O (can be programmed to be either input or output)</p> <p>As shown below, the gain option (A or B) must be set the same for both ports (0 & 1) via each port's IDX module.</p> <table border="1"> <thead> <tr> <th>TWO IDENTICAL PORTS (0 & 1)</th> <th>Option A: Both DRX16 IDX</th> <th colspan="2">Option B: Both DRX16 IDX-FG</th> </tr> </thead> <tbody> <tr> <td>Gain</td> <td>None on IDX modules</td> <td colspan="2">Fixed on IDX modules</td> </tr> <tr> <td>Frequency range</td> <td>2 to 300 MHz</td> <td colspan="2">2 to 300 MHz</td> </tr> <tr> <td>-3 dB bandwidth</td> <td>300 MHz</td> <td colspan="2">300 MHz</td> </tr> <tr> <td>Input impedance</td> <td>50 or optional 75 ohms</td> <td colspan="2">50 or optional 75 ohms</td> </tr> <tr> <td>Return loss</td> <td>16 dB</td> <td colspan="2">16 dB</td> </tr> <tr> <td>Signal level</td> <td>+4 dBm (max)</td> <td colspan="2">-40 to -20 dBm</td> </tr> <tr> <td>Typical SNR / SFDR</td> <td>70 / 75 dB</td> <td colspan="2">Maximum gain 55 / 45 dB; minimum gain 70 / 60 dB</td> </tr> </tbody> </table>			TWO IDENTICAL PORTS (0 & 1)	Option A: Both DRX16 IDX	Option B: Both DRX16 IDX-FG		Gain	None on IDX modules	Fixed on IDX modules		Frequency range	2 to 300 MHz	2 to 300 MHz		-3 dB bandwidth	300 MHz	300 MHz		Input impedance	50 or optional 75 ohms	50 or optional 75 ohms		Return loss	16 dB	16 dB		Signal level	+4 dBm (max)	-40 to -20 dBm		Typical SNR / SFDR	70 / 75 dB	Maximum gain 55 / 45 dB; minimum gain 70 / 60 dB	
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Timebase	10 MHz TCXO Frequency tolerance +/- 0.5 ppm at 25° C Frequency over temperature +/- 2.5 ppm at 0° to 75° C Impedance - Signal level - Return loss -	Reference input - - 50 ohms 0 to 7 usable (11 max) dBm 12 dB	Reference output - - 50 ohms 2 V peak to peak (ptp) -																																
Connectors	Both ports, SMB 50 or optional 75 ohms; sample clock I/O and both reference connectors, SMB 50 ohms; time code input, 7-pin Lemo																																		
Cabling	Consult EDT for purchase options: To 7-pin Lemo on board, from time code source	Via one DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only)																																	
Physical	Weight Dimensions	5.6 oz. typical 6.6 x 4.2 x 0.75 in. (with a main board)																																	
Environmental	Temperature (operating / non-operating) Humidity (operating / non-operating)	0° to 40° C / -40° to 70° C 1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C																																	
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.																																		

Ordering Options

- Main board: PCIe8 LX / FX / SX (required)
- DSP: Custom FPGA-based designs
- Gain: Option **A** / B (details above)
- Connectors (ports): **50** / 75 ohms
- Cabling (for time code input, if any): DB9 / BNC

Bold is default. For more options, see main board detail. **Ask** about custom options.