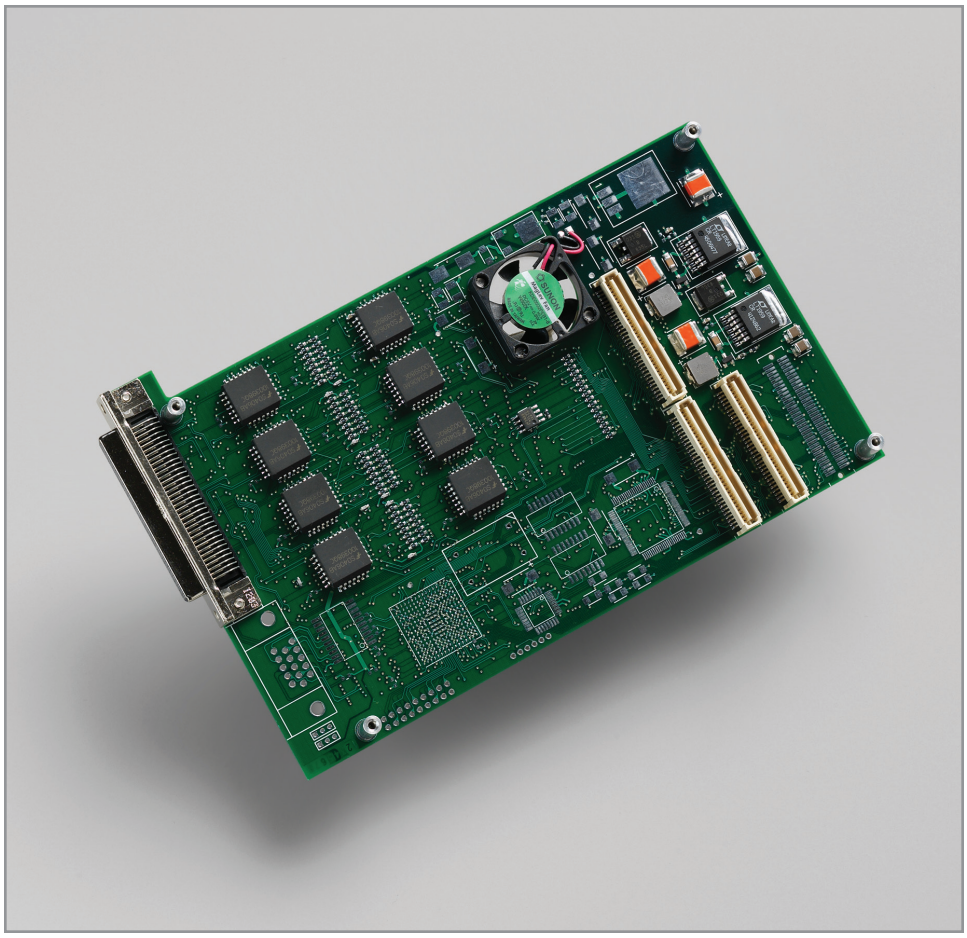
edt
a HEICO company

ECL / LVDS-E / RS422-E

Interface for ECL, LVDS, or RS422, with optional E1 (T1)



Features

- Mezzanine board – pairs with an EDT main board (PCI or PCIe), which adds DMA, programmable FPGA resources, and memory
- Clock: One external LVDS (input only)
- I/O (standard): ECL, LVDS, or RS422
- I/O (optional): Additional ECL or E1/T1

Description

The ECL/LVDS-E/RS422-E is a mezzanine board that pairs with a PCI / PCIe main board to provide fast, flexible data transfer. This "E-series" board supports thirty-two ECL, LVDS, or RS422 inputs or outputs in groups of four, with an option for additional ECL or E1/T1.

Each channel inputs or outputs a signal on the edge of the associated clock, and the data is stored in or sent from host memory via DMA for a simple, flexible data transfer solution.

Also available is an earlier "non-E" LVDS/RS422 board (identifiable by the absence of a fan), which does not support ECL or E1/T1 and works only with a PCI SS or PCI GS main board. Applications designed for this "non-E" board require different configuration files and minor program changes to work with the "E" board, as detailed in the user's guide.

EDT provides FPGA configuration files for all channels. Custom configuration files can be requested.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Applications

- Signal receiver and transmitter
- Communications monitoring (serial data)
- Satellite ground station support

Engineering Design Team, Inc. | 3423 NE John Olsen Ave. Hillsboro, Oregon 97124 USA | Tel: +1-503-690-1234 (800-435-4350) | Fax: +1-503-690-1243 | info@edt.com | edt.com

Specifications

Product Type	Interface for ECL, LVDS, or RS422, plus additional ECL or E1 (T1); it requires an EDT PCI / PCIe main board.			
FPGAs and Memory	Programmable FPGA and memory resources are provided by the main board.			
Clocks	One external LVDS (input only)			
Data Rates	Dependent on such factors as data format, main board, and system variables.			
Data Format (I/O)	One standard format (ECL, LVDS, or RS422) and one optional format (either additional ECL or E1/T1) are available, as shown below.			
	Standard (select ECL, LVDS, or RS422):	**ECL**	**LVDS**	**RS422**
	Independent I/O channels	16 (in groups of 4)	16 (in groups of 4)	16 (in groups of 4)
	Termination (differential)	50 ohms to -2 V DC	100 ohms line to line	100 ohms line to line
	Output jitter compliance	Yes	Yes	Yes
	Optional (select additional ECL or E1/T1 if desired):	**ECL**	**E1/T1**	
	Clock data I/O channels	See SSE datasheet*	16 (in groups of 4)	
	Transformer coupled	–	Yes	
	Compliance	–	G.703, T1.102	
	Mb/s	See SSE datasheet*	2.048 / 1.544	
	Coding	–	HDB3 / B8ZS	
	Jitter attenuation	–	Yes	
	*** NOTE:** This additional ECL option is the same as the ECL on EDT's SSE mezzanine board; for details, see SSE datasheet (catalog page).			
Connectors	One 68-pin AMP (SCSI 2-type) for ECL, LVDS, or RS422 One 15-pin D for E1/T1 option			
Cabling	Consult EDT for purchase options.			
Physical	Weight	3.3 oz typical		
	Dimensions	6.6 x 4.2 x 0.75 in. (with a main board)		
Environmental	Temperature (operating / non-operating)	0° to 40° C / -40° to 70° C		
	Humidity (operating / non-operating)	1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C		
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.			

Ordering Options

- Main board: PCI SS / GS or PCIe8 LX / FX / SX
- I/O (standard): ECL / LVDS / RS422
- I/O (optional): Additional ECL or E1/T1

For more options, see main board detail.
Ask about custom options.