

Net10G

Network processing interface for up to OC192/STM64 or 10GbE



Description

The Net10G is a dual-port mezzanine board that pairs with a PCI / PCIe main board to support multiple standards. It accepts electrical or optical ethernet of up to 10GbE, and also multiple SONET (SDH) signals.

The Net10G has two high-speed TCAMs and two pluggable form factors: one SFP for OC3/12/48 (STM1/4/16) or 1GbE (electrical or optical); and one XFP for OC192 (STM64) or 10GbE (electrical or optical). It has a programmable FPGA (Xilinx Virtex 5 LX), 2 GB of DRAM, and 8 MB of SRAM. It also has a time code input (IRIG-B or 1 pps) for timestamping.

EDT provides FPGA configuration files to support OC3/12/48/192 (raw, framed, framed and descrambled, header, and payload) and demultiplexing. Custom files can be requested.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Features

Mezzanine board – pairs with an EDT main board (PCI or PCIe), which adds DMA, programmable FPGA resources, and memory

Port 0: One optional SFP for 1GbE (electrical or optical) or OC3/12/48 (STM1/4/16) – 1550, 1310, or 850 nm

Port 1: One optional XFP for 10GbE (electrical or optical) or OC192 (STM64) – 1550, 1310, or 850 nm

Encoding: 8b/10b or 64b/66b

FPGA: One programmable Xilinx Virtex 5 LX XC5VLX110/220/330

SRAM: 8 MB (2 M x 36) for general use or TCAM-associated data

DRAM: 2 GB (DDR2) for snapshot recording and data buffering

TCAMs: Two (with lookup tables, configurable entries, and output tied to FPGA)

EDT intellectual property for 10GbE PMA and PCS layers and for SONET/SDH framing / demultiplexing

Time code input: 1 pps or IRIG-B, with user-configurable output

Applications

Multiple network data processing applications

Specifications

Product Type	Network processing interface for up to OC192/STM64 or 10GbE; it requires an EDT PCI / PCIe main board.			
FPGA Resources	One programmable FPGA (Xilinx Virtex 5 LX XC5VLX110 or optional 220 or 330), plus FPGA resources on main board			
Memory	SRAM	8 MB (2 M x 36) for general use or TCAM-associated data		
	DRAM (DDR2) for snapshot recording / data buffering	2 GB		
	TCAMs (with lookup tables and output tied to FPGA)	Two cascading, configurable 40-, 80-, 160-, 320-, or 640-bit entries		
Clocks	Programmable internal reference clock with jitter attenuation.			
Data Rates	Dependent on such factors as data format, main board, and system variables.			
Data Format (I/O)	Ethernet	SONET (SDH) – output can conform to SONET (SDH) to jitter specifications		
	Port 0: 1GbE (1000 BASE-T or -X)	OC3/12/48 (STM1/4/16)		
	Port 1: 10GbE (10G BASE-CX4 or -R)	OC192 (STM64)*		
	Also provided is a time code input (to connect to an external source) for 1 pps, IRIG-B, or other input, with user-configurable output.			
Transceivers	Two (port 0 has an optional SFP, while port 1 has an optional XFP) are available, supporting data as shown below.			
		ELECTRICAL	OPTICAL	
	Port 0 (1 SFP, optional)	1GbE	OC3/12/48 (STM1/4/16)	
	Output power	–	1550 nm	1310 nm
	Center wavelength	–	–2 to 3 dBm	–9.5 to –3 dBm
	Sensitivity	–	–9 to –2.5 dBm	–9 to –2.5 dBm
	Maximum input power	–	1500 to 1580 nm	1270 to 1360 nm
	Connector	RJ45	–28 dBm	–18 dBm
			–9 dBm	0 dBm
			0 dBm	0 dBm
			LC	LC
	Port 1 (1 XFP, optional)	10GbE	OC192 (STM64)	
	Output power	–	1550 nm	1310 nm
	Center wavelength	–	–1 to 2 dBm	–6 to –1 dBm
	Sensitivity	–	1550 nm	1290 to 1330 nm
	Maximum input power	–	–15 dBm	–13 dBm
	Connector	CX4rLC	–1 dBm	–0.5 dBm
			–1 dBm	–1 dBm
			LC	LC
Connectors	One 7-pin Lemo for time code input One RJ45, LC, or CX4 on each transceiver as shown above			
Cabling	Consult EDT for purchase options: To 7-pin Lemo on board, from time code source		Via one DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only)	
Physical	Weight	7.7 oz. typical		
	Dimensions	6.6 x 4.2 x 0.75 in. (with a main board)		
Environmental	Temperature (operating / non-operating)	0° to 40° C / –40° to 70° C		
	Humidity (operating / non-operating)	1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C		
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.			

Ordering Options

- Main board: PCI GS or PCIe8 LX / FX / SX
- FPGA: XC5VLX110 / 220 / 330
- Transceivers: 0, 1, or 2 [options above]
- Cabling (for time code input): DB9 / BNC

Bold is default. For more options, see main board detail. Ask about custom options.