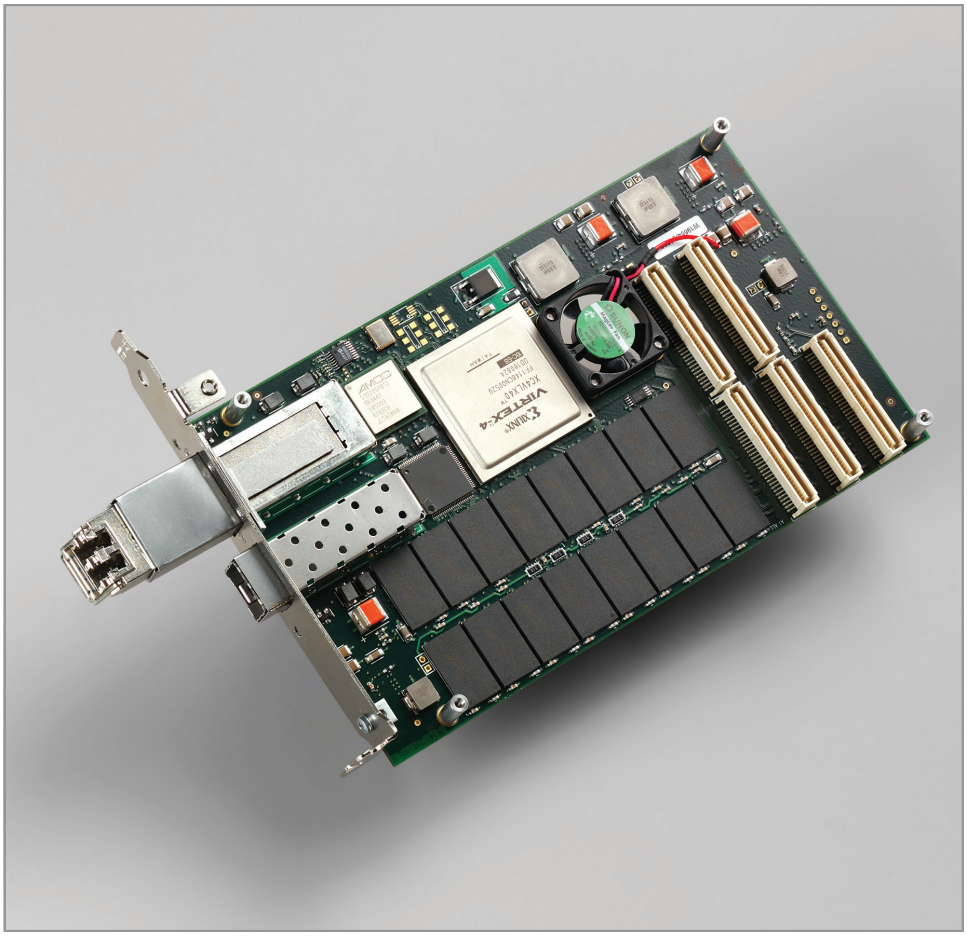
OC192

Optical carrier multirate interface for up to OC192 (STM64) / 10GbE



Description

The OC192 is a dual-port mezzanine board that pairs with a PCI / PCIe main board to support multiple standards.

Port 0 provides an optional SFP for 1GbE (optical or electrical), OTU1, or OC3/12/48 (STM1/4/16). Port 1 provides an XFP for 10GbE (optical or electrical), OTU2/2e, or OC192 (STM64).

The board has one programmable Xilinx Virtex 4 FPGA and 4 GB of DDR2 DRAM for snapshot recording and buffering.

EDT provides FPGA configuration files to support 1GbE and 10GbE (at the PHY layer); OC3/12/48/192 (raw, framed, framed and descrambled, header, and payload); OTU1/2/2e (raw, framed, framed and descrambled); and demultiplexing. Custom files can be requested.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Features

- Mezzanine board – pairs with an EDT main board (PCI or PCIe), which adds DMA, programmable FPGA resources, and memory
- Port 0: One optional SFP for 1GbE (electrical or optical), OTU1, or OC3/12/48 (STM1/4/16); optical signals can be 1550, 1310, or 850 nm
- Port 1: One XFP for 10GbE (electrical or optical), OTU2/2e, or OC192 (STM64); optical signals can be 1550, 1310, or 850 nm
- FPGA: One programmable Xilinx Virtex 4 LX XC4VLX40
- DRAM: 4 GB (DDR2) for snapshot recording and data buffering

Applications

- Telecommunications network monitoring
- Ethernet monitoring
- SONET/SDH to ethernet conversion

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Specifications

Product Type	Optical carrier multi-rate interface for up to OC192 (STM64) / 10GbE; it requires an EDT PCI / PCIe main board.
FPGA Resources	One programmable FPGA (Xilinx Virtex 4 LX XC4VLX40), plus FPGA resources on main board
Memory	DRAM (DDR2) — 4 GB for snapshot recording and buffering
Clocks (XO)	Port 0 can be set to: 125, 155.52, 156.25, or 166.62857 MHz Port 1 can be set to: 125, 155.52, 156.25, 166.62857, 161.13281, 167.33165, or 173.37075 MHz
Data Rates	Dependent on such factors as data format, main board, and system variables.

Data Format (I/O)

	1GbE (optical or electrical)	**10GbE (optical or electrical)**	**ITU-T G.709 (optical)**	**SONET (SDH) (optical)**
Port 0:	1000 BASE-T or -X	–	OTU1	OC3/12/48 (STM1/4/16)
Port 1:	–	10G BASE-CX4 or -R	OTU2/2e	OC192 (STM64)

Transceivers

Two (port 0 has an optional SFP, while port 1 has an included XFP) are available, supporting data as shown below.

	ELECTRICAL	**OPTICAL**		
Port 0 (1 SFP, optional)	**1GbE**	**1GbE, OTU1, or OC3/12/48 (STM1/4/16)**		
		1550 nm	**1310 nm**	**850 nm**
Output power	–	-2 to 3 dBm	-9.5 to -3 dBm	-9 to -2.5 dBm
Center wavelength	–	1500 to 1580 nm	1270 to 1360 nm	830 to 860 nm
Sensitivity	–	-28 dBm	-18 dBm	-18 dBm
Maximum input power	–	-9 dBm	0 dBm	0 dBm
Connector	RJ45	LC	LC	LC
Port 1 (1 XFP, included)	**10GbE**	**10GbE, OTU2/2e, or OC192 (STM64)**		
		1550 nm	**1310 nm**	**850 nm**
Output power	–	-1 to 2 dBm	-6 to -1 dBm	-3 to -1 dBm
Center wavelength	–	1550 nm	1290 to 1330 nm	850 nm
Sensitivity	–	-15 dBm	-13 dBm	-7.5 dBm
Maximum input power	–	-1 dBm	-0.5 dBm	-1 dBm
Connector	CX4	LC	LC	LC

Connectors	One RJ45, LC, or CX4 on each transceiver as shown above
Cabling	Consult EDT for purchase options.
Physical	Weight: 6.5 oz. typical Dimensions: 6.6 x 4.2 x 0.75 in. (with a main board)
Environmental	Temperature (operating / non-operating): 0° to 40° C / -40° to 70° C Humidity (operating / non-operating): 1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.

Ordering Options

- Main board: PCI GS or PCIe8 LX / FX / SX
- Transceivers: 1 or 2 [options above]

Bold is default. For more options, see main board detail. **Ask** about custom options.