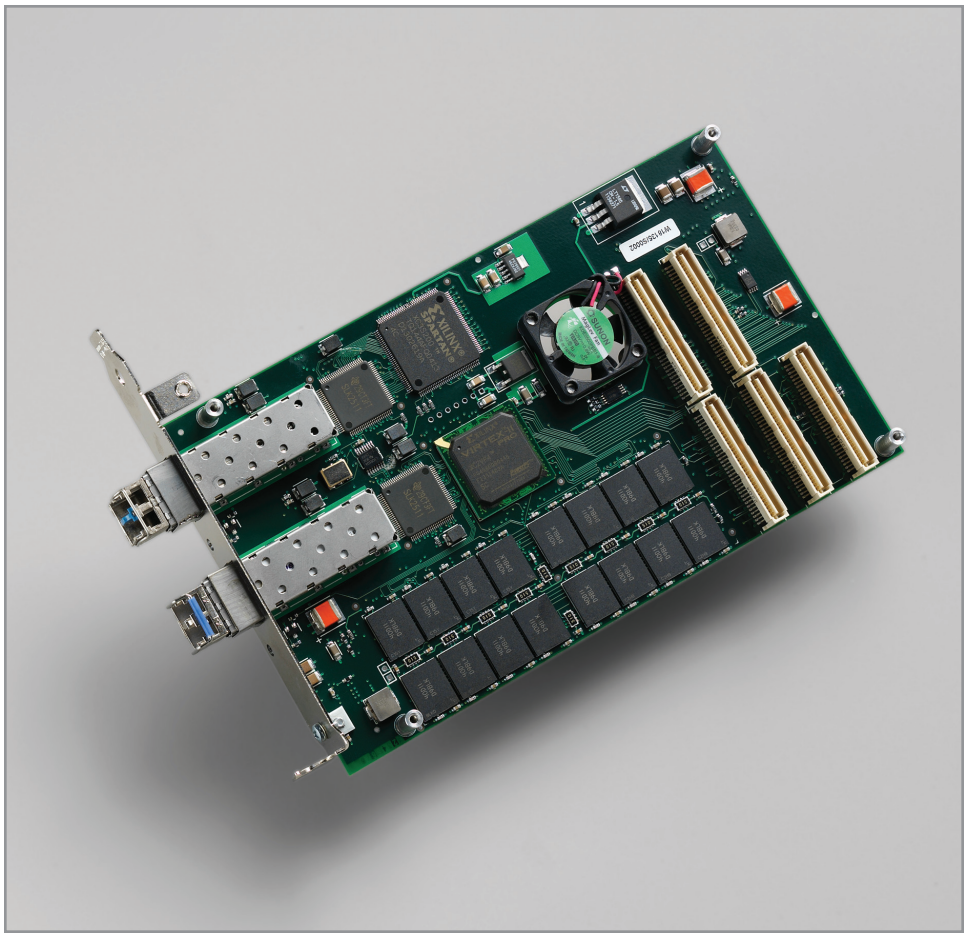
edt
a HEICO company

OCMP

Optical carrier multirate interface for up to OC48 (STM16) / 1GbE



Features

- Mezzanine board – pairs with an EDT main board (PCI or PCIe), which adds DMA, programmable FPGA resources, and memory
- Port 0: One SFP for 1GbE (optical or electrical) or OC3/12/48 (STM1/4/16) – 1310 nm; all are input and output
- Port 1: One SFP for 1GbE (optical or electrical) or OC3/12 (STM1/4) or OC3/12/48 (STM1/4/16) – 1310 nm; OC48 (STM16) is input only
- FPGAs: Two programmable (one Xilinx Spartan 3 XC3S200 and one Xilinx Virtex II Pro XC2VP4)
- DRAM: Up to 2 GB (DDR) for snapshot recording and data buffering
- Clocks: Two XOs (one per port) for internal reference, each independently programmable from 10 to 215 MHz

Description

The OCMP is a dual-port mezzanine board that pairs with a PCI / PCIe main board to support two small form pluggable (SFP) transceivers. Port 0 has an SFP to support 1GbE (electrical or optical) or OC3/12/48 (STM1/4/16) input and output. Port 1 has an SFP to support 1GbE or OC3/12 (STM1/4), with optional input-only support for OC48 (STM16).

Each port has a programmable Xilinx FPGA (port 0 has a Virtex II Pro, and port 1 has a Spartan 3) and a crystal oscillator (XO) for internal reference. The XOs can be programmed independently to any frequency from 10 to 215 MHz.

DRAM (up to 2 GB) is included for snapshot recording and data buffering.

EDT provides FPGA configuration files to support 1GbE (at the PHY layer) and OC3/12/48/192 (raw, framed, framed and descrambled, header, and payload). Custom configuration files can be requested.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Applications

- Telecommunications network monitoring
- Ethernet monitoring
- SONET/SDH to ethernet conversion

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Specifications

Product Type	Optical carrier multirate interface for up to OC 48 (STM16) / 1 GbE; it requires an EDT PCI / PCIe main board.			
FPGA Resources	Two programmable FPGAs (plus FPGA resources on main board): Port 0 Port 1		One Xilinx Virtex II Pro XC2VP4 One Xilinx Spartan 3 XC3S200	
Memory	DRAM (DDR) for snapshot recording / data buffering		0 or optional 512 MB or 2 GB; 2 GB is needed for snapshot recording at rates of OC48/STM16 or faster with PCI SS or PCI GS main board	
Clocks	Two XOs (one per port, for internal reference)		Either can be programmed to any frequency from 10 to 215 MHz	
Data Rates	Dependent on such factors as data format, main board, and system variables.			
Data Format (I/O)		**Ethernet**	**SONET (SDH)**	
	Port 0:	1GbE (1000 BASE-T or -X)	OC3/12/48 (STM1/4/16)	
	Port 1:	1GbE (1000 BASE-T or -X)	OC3/12 (STM1/4), with optional input-only OC48 (STM16)	
Transceivers	Two (port 0 and 1 each have one) are included, supporting data as shown below.			
		ELECTRICAL	**OPTICAL**	
	PORT 0 **(1 SFP, included)**	**1GbE**	**1GbE or** **OC3/12 (STM1/4) plus input-output OC48 (STM16)** **1310 nm**	
	Output power	–	–9.5 to –3 dBm	
	Center wavelength	–	1270 to 1360 nm	
	Sensitivity	–	–18 dBm	
	Maximum input power	–	0 dBm	
	Connector	RJ45	LC	
	PORT 1 **(1 SFP, included)**	**1GbE**	**Standard: 1GbE or** **OC3/12 (STM1/4)** **1310 nm**	**Optional: 1GbE or** **OC3/12 (STM1/4) plus input-only OC48 (STM16)** **1310 nm**
	Output power	–	–15 to –8 dBm	–9.5 to –3 dBm
	Center wavelength	–	1270 to 1360 nm	1270 to 1360 nm
	Sensitivity	–	–28 dBm	–18 dBm
	Maximum input power	–	0 dBm	0 dBm
	Connector	RJ45	LC	LC
Connectors	One RJ45 or LC on each transceiver as shown above.			
Cabling	Consult EDT for purchase options.			
Physical	Weight Dimensions		3.5 oz. typical 6.6 x 4.2 x 0.75 in. (with a main board)	
Environmental	Temperature (operating / non-operating) Humidity (operating / non-operating)		0° to 40° C / -40° to 70° C 1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C	
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board			

Ordering Options

- Main board: PCI SS / GS or PCIe8 LX / FX / SX
- Memory – DRAM: **0** / 512 MB / 2 GB
- Transceivers: 2 [options above]

Bold is default. For more options, see main board detail. **Ask** about custom options.