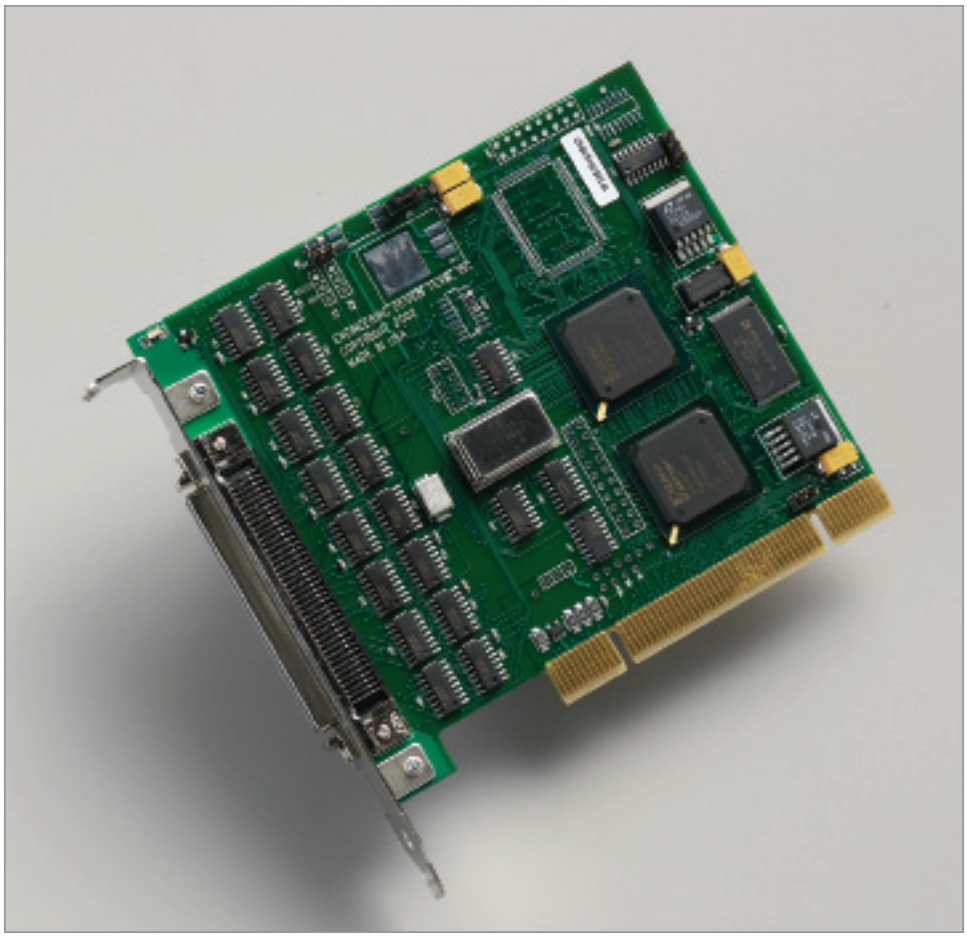
edt
a HEICO company

PCI CD/a

PCI interface for configurable DMA and synchronous I/O



Features

PCI interface for high-speed DMA (one or sixteen channels) and synchronous RS422 or LVDS I/O (one, two, eight or sixteen channels)

Supports one, two, eight, or sixteen channels of differential data:
- One 16-bit parallel;
- Two 8-bit parallel (full duplex);
- Eight synchronous serial with data valid; or
- Sixteen synchronous serial

FPGA: One user-programmable Xilinx Spartan IIE
- Standard XC2S100E for one or two data channels; or
- Optional XC2S600E for eight or sixteen data channels

I/O: RS422 or LVDS

Buffers: Integrated FIFOs for input and output

Clock: 33 or 66 MHz, 3- or 5-volt PCI-capable

Data rates:
- With one DMA channel, 210 MBytes per second
- With sixteen DMA channels, 70 Mbits per second per channel

Description

The PCI CD/a is a PCI interface that provides fast DMA and synchronous I/O to transfer differential data (RS422 or LVDS) between an external device and a host computer.

The board provides two FPGA options (Xilinx Spartan IIE) to enable one or multiple differential data channels. The standard FPGA (XC2S100E) enables one 16-bit parallel channel, or two 8-bit parallel full duplex channels. The optional FPGA (XC2S600E) enables eight synchronous serial channels with data valid, or sixteen synchronous serial channels.

Per-second data rates (observed) are up to 210 MBytes for one DMA channel, or 70 Mbits per channel for sixteen DMA channels.

The hardware protocol is synchronous: all data and control signals are sampled by a clock transmitted along with them. This sample clock can be generated by the DMA interface, the user device, or both.

All data channels are VHDL in the user-interface FPGA. EDT provides access to the source VHDL for custom designs.

Applications

Simulation

Imaging devices

Scanners

Plotters

Device control

General-purpose data acquisition

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Specifications

Product Type	PCI CD/a is a PCI interface that provides high-speed DMA and synchronous I/O for RS422 or LVDS.	
FPGA Resources	One programmable Xilinx Spartan IIE, which can be either of these:	
	Standard XC2S100E	For one or two data channels
	Optional XC2S600E	For eight or sixteen data channels
Other Resources	Buffers	Integrated FIFOs for input and output
Memory	0	
Clock	1 PLL clock generator	66 or 33 MHz, 3- or 5-volt PCI-capable
Data Rates	For one-channel operation	210 MBytes per second
	For optional sixteen-channel operation	70 Mbits per second per channel
Data Format (I/O)	RS422 or LVDS	
PCI Compliance	PCI version	PCI 2.3
	DMA	One or sixteen channels
	Number of slots	One
Connectors	One AMP 787190-8 high-density 80-pin (mates with AMP 749621-8, backshell 749196-2)	
Physical	Weight	3.3 oz. typical
	Dimensions	5.0 x 4.2 x 0.5 in.
Environmental	Temperature	Operating: 10° to 40° C
		Non-operating: -40° to 70° C
	Humidity	Operating: 1% to 90%, non-condensing at 40° C
		Non-operating: 95%, non-condensing at 40° C
System and Software	System must have a PCI or PCI-X bus, 66 MHz or faster (33 MHz will work, but at reduced data rates). Software is included for Windows, Linux, and Mac OS X; for versions, see our website.	

Ordering Options

Part number	Description
019-01854 / -11854	LVDS with 100E FPGA
019-01960	RS422 with 100E FPGA
019-02039	LVDS with 600E FPGA
019-02216	LVDS with 600E FPGA + SSD16 configuration file
019-02219 / -12219	RS422 with 600E FPGA
019-02234	RS422 with 600E FPGA + SSD16 configuration file
019-14879	LVDS with 100E FPGA + SSD16 configuration file