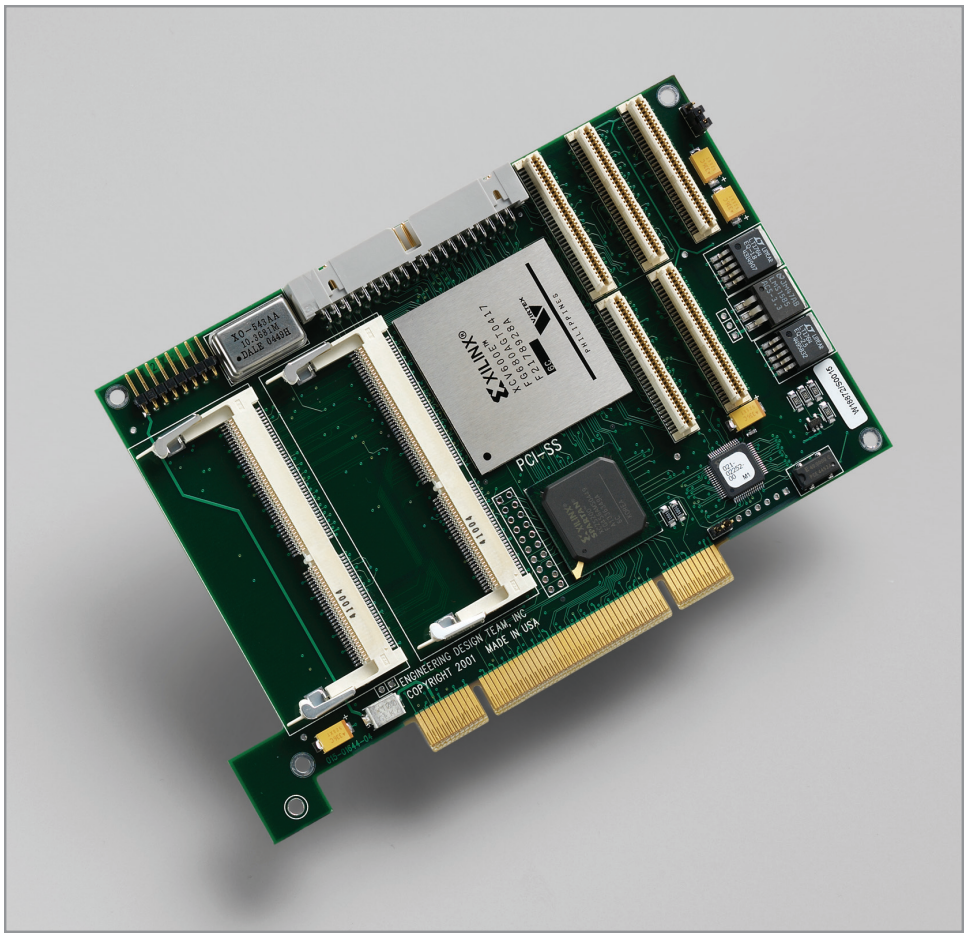
edt
a HEICO company

PCI SS

PCI DMA and data processing interface



Description

The PCI SS is a PCI main board that provides DMA, memory, and FPGA resources to a mezzanine board.

The PCI SS has a programmable FPGA (Xilinx Virtex-E XCV1000E or optional 2000E or 600E) and synchronous memory of up to 8 MB SRAM.

The board also has four independent programmable PLL clock generators, which can be set to select frequencies with less than +/- 50 ppm error.

The board is designed to work with numerous EDT mezzanine boards. An EDT Bridge can be ordered to link two main boards together.

Applications

EDT mezzanine board support for PCI or PCI-X form factors

Features

- Main board (PCI) – provides an EDT mezzanine board with DMA, programmable FPGA resources, and memory
- 221 LVTTL programmable signals connected to mezzanine board
- FPGA: One programmable Xilinx Virtex-E (XCV1000E or optional 2000E or 600E)
- SRAM: Up to 8 MB
- Clocks: Four independent programmable PLL clock generators

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Specifications

Product Type	PCI main board; it supplies DMA, memory, and FPGA resources to a mezzanine board.	
FPGA Resources	One programmable FPGA (Xilinx Virtex-E XCV1000E or optional 2000E or 600E)	
Memory	SRAM (with HRC or OCMP mezzanine board)	One bank of 256 K x 36 (1 MB total) or optional 512 K x 36 (2 MB total) or optional 1 M x 36 (4 MB total) or optional 0
	SRAM (with any other mezzanine board)	Two banks of 256 K x 36 (1 MB per bank; 2 MB total) or optional 512 K x 36 (2 MB per bank; 4 MB total) or optional 1 M x 36 (4 MB per bank; 8 MB total) or optional 0
	DRAM	0
Clocks	Four programmable independent PLL clock generators, each with input and output clocks: Input (reference) clocks can be set to 10.3681 or 40 MHz, or PCI clock. Output clocks can be set with only +/- 50 ppm error to 1.544, 2.048, 6.312, 8.448, 34.368, or 44.736 MHz.	
Data Rates	Dependent on such factors as data format, mezzanine board, and system variables.	
Data Format (I/O)	Determined by mezzanine board and auxiliaries	
PCI Compliance	PCI version DMA Number of slots	PCI 2.3 1, 4, or 16 channels, depending on mezzanine board 1
Connectors	Five CMC-type (IEEE 1386) mezzanine One 8-pin .100" x 1 row square .025" square pins One 40-pin ATA-type expansion	221 LVTTL I/O (mate to AMP 120527-1 or Molex 71436-2164) For six external debugging LEDs 30 LVTTL signals for external board or FPGA debugging
Cabling	Consult EDT for purchase options.	
Physical	Weight Dimensions	3.3 oz. typical 6.6 x 4.2 x 0.75 in.
Environmental	Temperature (operating / non-operating) Humidity (operating / non-operating)	0° to 40° C / -40° to 70° C 1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C
System and Software	System must have a PCI or PCI-X bus, 66 MHz or faster (33 MHz will work, but at reduced data rates). Software is included for Windows and Linux, with limited support for Solaris and Mac OS; for versions, see www.edt.com.	

Ordering Options

- Mezzanine board: See Compatibility Guide.
- FPGA: XCV**1000E** / 2000E / 600E
- Memory – SRAM: Up to 8 MB [options above]

Bold is default. For more options, see mezzanine board detail. **Ask** about custom options.