edt
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PCIe8 DV/DVa C-Link

PCIe x8 digital video Camera Link interface

Description

The PCIe8 DV/DVa C-Link is a PCIe x8 Camera Link interface that provides uncompressed image capture for digital video. It has two MDR26 connectors to support one full-, one medium-, or up to two base-mode cameras.

The board fits in an 8- or 16-lane PCIe slot. Images of any resolution are captured and displayed, in real time, via DMA to the host computer; speed, resolution, and buffers are limited only by host bandwidth and memory. Optional 1 GB DDR2 provides snapshot recording and frame buffering.

Line and frame triggering are supported over camera control lines, while onboard UART provides serial control. External triggering and timecode input (IRIG-B) are enabled by the provided Berg or the optional Lemo connector.

Provided with the board are drivers for supported operating systems and a software development kit that includes C language libraries, examples, utilities, image capture and display GUI, camera configuration files, and Camera Link standard DLL for camera control.

Features

- Camera Link interface fits in an 8- or 16-lane PCIe slot
- Supports one full-, one medium-, or up to two base-mode cameras
- Provides frame storage and buffering via optional 1 GB DDR2
- Captures and displays images in real time, via DMA to host computer
- Provides onboard region-of-interest control
- Supports line and frame triggering over camera control lines
- Offers optional timecode input (IRIG-B) for precise timestamping
- Supports data rates up to 1.2 GB/s

Applications

- Astronomy / biology / microscopy
- Aerial mapping / traffic systems
- Commercial film / multimedia
- Medical and nuclear imaging
- Remote scientific monitoring
- Manufacturing / inspection
- Machine vision / robotics
- Security / surveillance
- Scanning / archiving

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Specifications

Memory	FIFO DDR2 (SODIMM)	Up to several lines of data 0 or optional 1 GB
Data Rates	Peak / typical	1.2 GB/s / 850 MB/s (or maximum supported by host)
Data Format (I/O)	Camera Link input; timecode input (IRIG-B)	
Camera Link Compliance	Camera Link version Power over Camera Link (PoCL) Modes Pixel clock rate Serial CC1 - CC4 Connectors	2.0 Selected by jumpers, polyswitch protected Base, dual base, medium, full — common configurations Base—medium mode, 20—85 MHz; full—extended full mode, 30—85 MHz Via API or serial DLL (9600 to 115,200 baud) Discretely programmable for steady-state, trigger, and timed pulse Two MDR26 for data and control
EU Compliance	CE RoHS WEEE	Contact EDT Contact EDT Contact EDT
PCI Express Compliance	PCIe version Direct memory access (DMA) Number of lanes	PCIe 1.1 Yes 8
Noise	0 dB	
MTBF	Estimated at 200,000 hours	
Triggering	Via CC lines, or externally via connector (opto-coupled Berg or optional 7-pin Lemo — mate to FGG.0B.307.CLAD.56)	
Connectors	Two MDR26 Camera Link One opto-coupled Berg One optional 7-pin Lemo	For data and control For external triggering, timecode input (IRIG-B), or both For external triggering, timecode input (IRIG-B), or both
Cabling	Cabling is purchased separately; consult EDT for options.	
Physical	Weight Dimensions	3.5 oz. typical 4.8 x 4.8 x 0.7 in.
Environmental	Temperature (operating / non-operating) Humidity (operating / non-operating)	10° to 40° C / -20° to 60° C 1% to 90% non-condensing at 40° C / 95% non-condensing at 45° C
System and Software	System must have a PCI Express bus (8 or 16 lanes) that is not dedicated to display use only. Software is included for Windows and Linux; for versions, see edt.com.	

Ordering Options

- Memory - DDR2 (SODIMM): **0** / 1 GB
- Connector: **Berg (included)** / Lemo (optional), for external triggering, IRIG-B input, or both

Bold is default. **Ask about custom options.**