

PCIe8 DV/DVa CLS

PCIe x8 digital video Camera Link simulator



Description

The PCIe8 DV/DVa CLS is a PCIe x8 Camera Link simulator that generates image data by simulating one extended full, full, or medium mode camera, or up to two base-mode cameras. It provides a pixel clock rate of 20 to 85 MHz (in increments of 0.25 MHz) and a text-based configuration script, easily modifiable to match the timing parameters of the camera to be simulated.

The board fits in an 8- or 16-lane PCIe slot. Known image data allows easy debug of interface application code, and system debug when target camera is unavailable.

Images are sent via DMA from host memory as required by the application. Internal counters can be used an alternate source of image data. Optional 1 GB DDR2 provides frame buffering.

Line and frame triggering are supported over camera control lines.

C language libraries allow the user to define appropriate responses to UART commands from the interface.

The PCIe8 DVa CLS is shipped as a simulator; however, with a simple firmware reload and power cycle, it converts to a PCIe8 DVa C-Link framegrabber. Once converted, it then operates as specified on the PCIe8 DVa C-Link datasheet.

In framegrabber mode, external triggering and timecode input (IRIG-B) are enabled by the provided Berg or the optional Lemo connector.

Features

- Camera Link simulator fits in an 8- or 16-lane PCIe slot
- Simulates Camera Link digital cameras, base through extended full mode, 1 to 10 taps; supports two base mode outputs at same frequency
- Provides frame storage and buffering via optional 1 GB DDR2
- Supports DMA from host memory for image data
- Allows internal counters to be used as alternate source of image data
- Allows emulation of camera UART commands
- Supports line and frame triggering over camera control lines
- Converts to framegrabber via a simple firmware reload and power cycle
- Optional 7-pin Lemo supports external triggering or IRIG-B timecode input (framegrabber mode only)
- Supports pixel clock rate of 20 to 85 MHz in increments of 0.25 MHz

Applications

Any PCIe application requiring simulated Camera Link output

Specifications

| | | |
|--|--|---|
| Memory | FIFO DDR2 (SODIMM) | Up to several lines of data 0 or optional 1 GB |
| Clock | Camera Link | 20–85 MHz (in increments of 0.25 MHz) – both channels at same frequency |
| Data Format (I/O) | In simulator mode In framegrabber mode | Camera Link output (simulated) Camera Link input; timecode input (IRIG-B) |
| Camera Link Compliance (simulator mode) | Modes Pixel clock rate (in increments of 0.25 MHz) Serial CC1 - CC4 Connectors | Base, dual base, medium, full, extended full – common configurations NOTE: In dual base mode, both channels must be at same frequency. Base–extended full mode (in development), 20–85 MHz 9600 to 115,200 baud (via API or serial DLL) Discretely programmable for steady-state, trigger, and timed pulse Two MDR26 for data and control |
| Camera Link Compliance (framegrabber mode) | Modes Pixel clock rate (in increments of 0.25 MHz) Serial CC1 - CC4 Connectors | Base, dual base, medium, full, extended full – common configurations Base–medium mode, 20–85 MHz; full mode, 30–85 MHz 9600 to 115,200 baud (via API or serial DLL) Discretely programmable for steady-state, trigger, and timed pulse Two MDR26 for data and control |
| EU Compliance | CE RoHS WEEE | Contact EDT Contact EDT Contact EDT |
| PCI Express Compliance | PCIe version Direct memory access (DMA) Number of lanes | PCIe 1.1 Yes 8 |
| Noise | 0 dB | |
| MTBF | Estimated at 200,000 hours | |
| Triggering | Freerun or via CC lines (programmable) or, in framegrabber mode, externally via connector (opto-coupled Berg or optional Lemo) | |
| Connectors | Two MDR26 Camera Link One opto-coupled Berg One optional 7-pin Lemo | For data and control In framegrabber mode: For external triggering, timecode input (IRIG-B), or both In framegrabber mode: For external triggering, timecode input (IRIG-B), or both |
| Cabling | Cabling is purchased separately; consult EDT for options. | |
| Physical | Weight Dimensions | 3.5 oz. typical 4.8 x 4.8 x 0.7 in. |
| Environmental | Temperature (operating / non-operating) Humidity (operating / non-operating) | 10° to 40° C / -20° to 60° C 1% to 90% non-condensing at 40° C / 95% non-condensing at 45° C |
| System and Software | System must have a PCI Express bus (16 or 8 lanes, or an 8-lane physical slot wired as a 4-lane with reduced maximum performance) that is not dedicated to display use only. Software is included for Windows and Linux; for versions, see edt.com. | |

Ordering Options

- Memory – DDR2 (SODIMM): **0** / 1 GB
- Connector: **Berg (included)** / Lemo (optional), for external triggering, IRIG-B input, or both [in framegrabber mode only]

Bold is default. **Ask about custom options.**