PCIe8g3 KU-10G

PCIe Gen3 x8 board: Kintex Ultrascale FPGA and 10G SFP/+s

Includes active FPGA heat sink (not shown).

Features

- PCIe (Gen3) x8 interface with up to four 10G SFP/+s
- Data formats: 1/10GbE, OC3/12/48/192 (STM1/4/16/64), OTU1/2/2e/2f
- FPGA (UI): One user-configurableXilinx Kintex Ultrascale (035, 060, 085, 115)
- FPGA (PCIe): One (up to 16 DMA channels via EDT FPGA configuration files)
- DRAM (DDR3): Two independent 64-bit blocks of 2 GB each (4 GB total)
- EDT intellectual property for 10GbE PCS and PMA layers, SONET/SDH framing, demultiplexing, and G.709 framing
- Optional Lemo for time code input, with user-configurable output

Description

The PCIe8g3 KU-10G is a fast, versatile PCI Express (PCIe, Gen3) x8 interface with up to four 10G SFP/+ ports. It supports 1/10GbE, OC3/12/48/192 (STM1/4/16/64), or OTU1/2/2e/2f.

Each port links to the user-interface (UI) FPGA for serialization / deserialization (SERDES) and clock recovery. Each port has its own reference clock, programmable for 10–210 MHz.

The UI FPGA is a Xilinx Kintex Ultrascale (U035, 060, 085, or 115) with access to two independent 64-bit wide blocks (2 GB each, 4 GB total) of DDR3 DRAM which can act as data buffers. This UI FPGA configures from flash at power-on, and can be reconfigured as many times as desired without powercycling. Up to five images are available, depending on which UI FPGA model is used.

The PCIe FPGA provides up to 16 independent DMA channels via EDT FPGA configuration files.

An optional Lemo supports time code input (1 pps or IRIG-B), with user-configurable output and two cabling options.

EDT provides FPGA configuration files to support 1GbE and 10GbE at the PHY layer; OC3/12/48/192 and OTU1/2/2e/2f (raw, framed, framed and descrambled); and demultiplexing. Custom files can be requested.

Applications

- Telecommunications monitoring, recording, and processing
- SONET/SDH to ethernet conversion
- Multiple other network processing applications

EDT, Inc. | 1400 NW Compton Drive, Suite 315 | Beaverton, Oregon 97006 USA | Tel: +1-503-690-1234 (800-435-4350) | Fax: +1-503-690-1243 | info@edt.com | edt.com

Specifications

Product Type	PCIeGen3 x8 board: Kintex Ultrascale FPGA; 1–4 10G SFP/+s for up to 10GbE / OC192 (STM64) / OTU2f.
FPGA Resources + DMA	UI FPGA (user-configurable): 1 Kintex Ultrascale (U035, U060, U085, or U115) PCIe FPGA: 1 Altera Arria V GZ for up to 16 independent DMA channels
Memory	DDR3 DRAM, two independent blocks of 2 GB (4 GB total); each block is 64 bits wide - for snapshot recording / data buffering
Clocks (Reference)	Up to four (one per port), each independently programmable from 10 to 210 MHz with limited support for reference loop timing.
Data Rates	Dependent on such factors as data format, main board, and system variables.
Data Format (I/O)	Via multiple ports, the board supports various data formats as shown below: 1/10GbE, OC3/12/48/192 (STM1/4/16/64), OTU1/2/2e/2f). Also provided is a time code input (to connect to an external source) for 1 pps, IRIG-B, or other input, with user-configurable output.
Transceivers	The board has multiple transceiver options, as shown below.

Up to four SFP/+*	**ELECTRICAL (1GbE)**	**OPTICAL (10GbE) SFP/+***	**SFP/+***	**SFP/+***
		1550 nm	**1310 nm**	**850 nm**
Output power (dBm)	–	–2 to +3 / 0 to +4	–9.5 to –3 / –8.2 to +0.5	–9 to –2.5 / –5 to –1
Center wavelength (nm)	–	1500–1580 / 1530–1565	1270–1360 / 1260–1355	830–860 / 840–860
Sensitivity (dBm)	–	–28 / –23	–18 / –10.3	–18 / –7.5
Max input power (dBm)	–	–9 / –7	0 / +0.5	0 / +0.5
Connector	RJ45 transceiver	LC	LC	LC

* An **SFP** at 1550, 1310, or 850 nm can support 1GbE, OC3/12/48 (STM1/4/16), or OTU1.
An **SFP+** at 1550 or 1310 nm can support 10GbE, OC192 (STM64), or OTU2/2e/2f — or, at 850 nm, 10GbE only.

Cooling	Active heat sink
Connectors	One optional 7-pin Lemo for time code input (1 pps or IRIG-B) with user-configurable output One RJ45 or LC on each SFP/+ as shown above
Cabling	For optional time code input, from source to Lemo: One DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only) For other cabling, consult EDT for purchase options.
Physical	Weight: 8.6 oz. (with active heat sink, but without transceivers) Dimensions: 6.6 x 4.2 x 0.75
Environmental	Temperature (operating / non-operating): 0° to 40° C / -40° to 70° C Humidity (operating / non-operating): 1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C
System and Software	System must have a PCI Express bus (8 or 16 lanes) that is not dedicated to display use only. Software is included for Windows and Linux; for versions, see www.edt.com.

Ordering Options

- FPGA: U035 / U060 / U085 / U115
- Transceivers: [options above]
- Optional time code input:
  - 1 Lemo connector + cabling (DB9 or BNC)

Bold is default. For more options, see main board detail. **Ask** about custom options.