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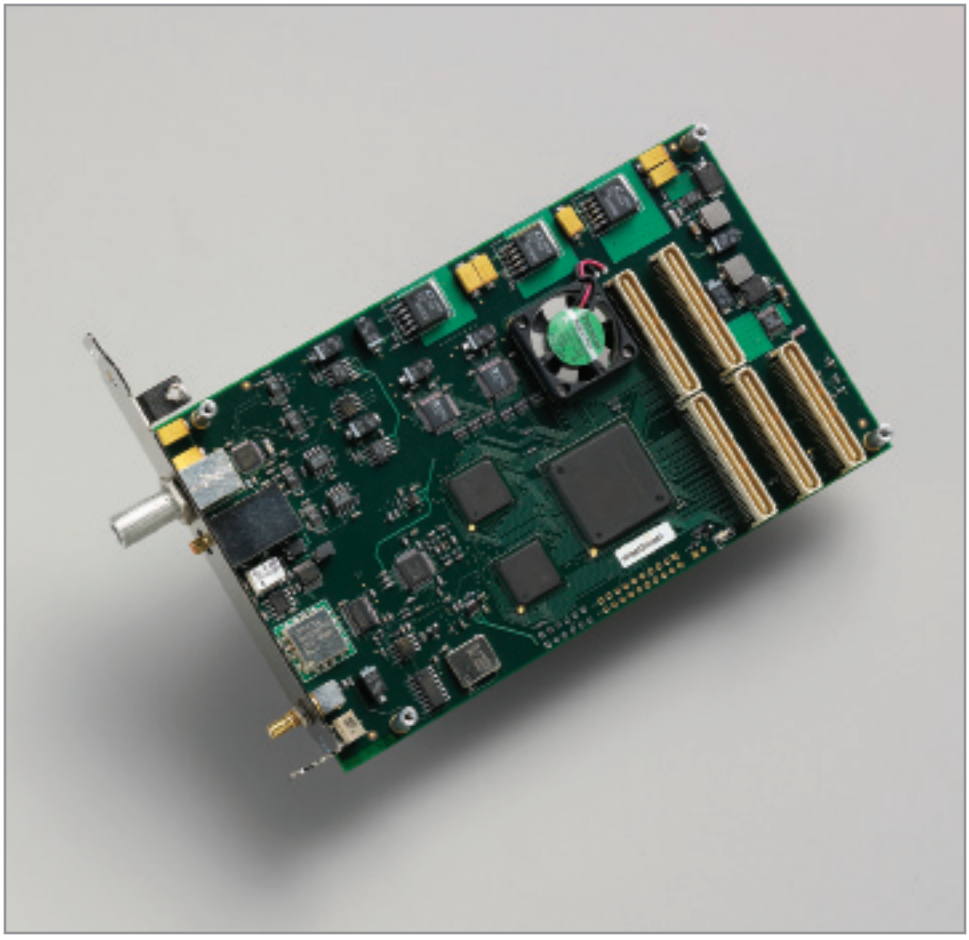
SRXL

Signal receiver and processor for IF and L-band



Description

The SRXL is a mezzanine board that pairs with a PCI / PCIe main board to accept simultaneous RF inputs in the L-band range of 925 to 2175 MHz and the IF range of 65 to 225 MHz.

Each input is processed with a tunable quadrature down-converter. The resulting baseband I and Q signals are low-pass filtered and digitized with 12-bit precision at programmable sample rates up to 65 MHz.

The resulting four sample data streams are available as inputs to the Xilinx Spartan 3 FPGA, which is programmable to perform signal processing or to serve as a configurable switch matrix to route data to the main board and two Graychips (GC4016), each with four digital down-convertors.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Features

- Mezzanine board – pairs with an EDT main board (PCI or PCIe), which adds DMA, programmable FPGA resources, and memory
- Simultaneous L-band and IF analog-to-digital conversion (12-bit)
- L-band: 925 to 2175 MHz (66 MHz bandwidth) with 5 MHz tuning resolution
- IF: 65 to 225 MHz (46 MHz bandwidth) with 1 MHz tuning resolution
- FPGA: One programmable Xilinx Spartan 3 XC3S1500
- Graychips: Two (TI GC4016), each with four DDCs
- Sample clock: Programmable to any frequency from 1 to 65 MHz
- Timebase: 10 MHz TCXO or user input

Applications

- Satellite receiver
- Software-defined radio
- Surveillance / spectrum monitoring
- Digital tuning
- Test and measurement equipment

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Specifications

Product Type	Signal receiver interface for IF and L-band; it requires an EDT PCI / PCIe main board.		
FPGAs and Memory	One programmable FPGA (Xilinx Spartan 3 XC3S1500), plus FPGA and memory resources on main board		
Graychips	Two programmable (TI GC4016)		
Sample Clock	User-configurable & phase-locked to 10 MHz reference	Tuning range = 1 to 6 MHz; tuning word (DDS) = 32 bits	
ADCs (one per port)	Two dual ADCs (one per port); resolution / maximum sample rate = 12 bits / 65 MHz		
Data Rates	Dependent on such factors as data format, main board, and system variables.		
Data Format (I/O)	Two inputs are included, supporting the data formats shown below. (For external reference input, see next heading.)		
	Radio frequencies (RFs):	**L-band (925-2175 MHz,**	**IF (65-225 MHz,**
	General	**5 MHz tuning resolution)**	**1 MHz tuning resolution)**
	Nominal input impedance	75 ohms	75 ohms
	Minimum return loss	12 dB	12 dB
	Gain control		
	Minimum RF	60 dB	-
	Minimum base band	19 dB	-
	Minimum variable	-	43 dB
	Typical variable	-	60 dB
	Signal level		
	Minimum usable	–72 dBm	–76 dBm
	Maximum usable	3 dBm	–19 dBm
	Absolute maximum	10 dBm	10 dBm
	Phase noise		
	At 40 KHz (measured)	-72 dB	-72 dB
	At 10 KHz (measured)	-50 dB	-65 dB
	Local Oscillators		
	Tuning ranges	925 to 2175 MHz	63 to 112 MHz or 125 to 225 MHz
	Tuning step size	5 MHz	1 MHz
	Demodulators		
	Base band LP filter cutoff	4 to 33 MHz (–3 dB)	23 MHz
	Transition band	42 dB/octave	24 dB/octave
	Maximum IQ phase error	4 degrees	3 degrees
	Maximum IQ gain error	1.2 dB	0.6 dB
External Reference	**10 MHz (input):** Impedance 50 ohms; return loss 12 dB; signal level -10 to 10 dBm usable (16 dBm maximum)		
Internal Reference	**10 MHz (TCXO):** Frequency adjustment range +/– 3 ppm; tolerance +/– 0.5 ppm at 25° C; over temperature +/– 2.5 ppm at 0° to 75° C		
Connectors	For external reference, SMB 50 ohms; for L-band, F-type 75 ohms; for IF, SMB 75 ohms		
Cabling	Consult EDT for purchase options.		
Physical	Weight	3.6 oz. typical	
	Dimensions	6.6 x 4.2 x 0.75 in. (with a main board)	
Environmental	Temperature (operating / non-operating)	0° to 40° C / -40° to 70° C	
	Humidity (operating / non-operating)	1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C	
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.		

Ordering Options

- Main board: PCI SS / GS or PCIe8 LX / FX / SX

Bold is default. For more options, see main board detail. **Ask** about custom options.