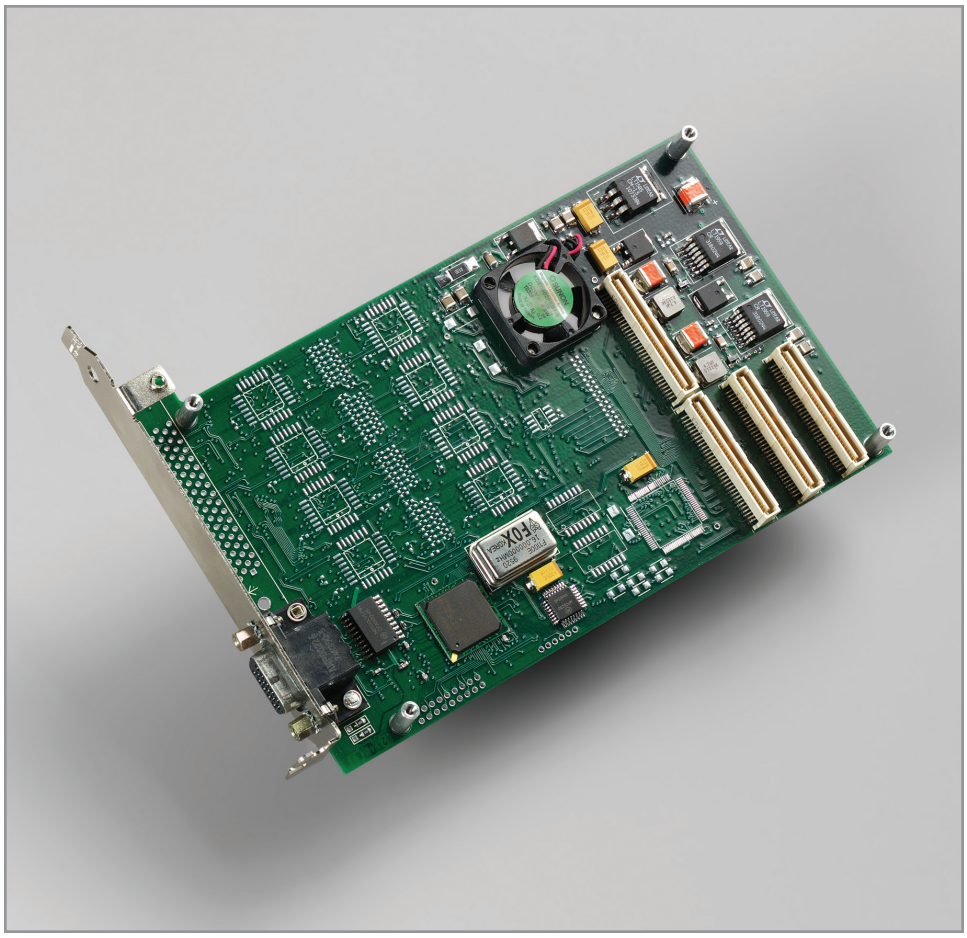
edt
a HEICO company

SSE

Synchronous serial ECL interface



Features

- Mezzanine board – pairs with an EDT main board (PCI or PCIe), which adds DMA, programmable FPGA resources, and memory
- Ports 0 and 1 (input) and Port 2 (output): One ECL data bit per port
- Clocks: Ports 0 and 1 each can receive, and port 2 can generate locally, a clock of up to 300 MHz for Reed-Solomon or 400 MHz for raw serial data
- FPGAs: One programmable Xilinx Virtex II Pro (XC2VP2 or XC2VP4)
- Reed-Solomon coding or raw serial data (with frame synchronization or not)
- Two user-defined LEDs

Description

The SSE is a mezzanine board that pairs with a PCI / PCIe main board to provide fast data transfer. It supports two input ports and one output port of ECL (with one ECL data bit per port).

The SSE samples the data on the rising edge of the clock and stores it in host memory via the main board. Each port has two wires to support one differential data signal, and two more wires to support one differential clock signal. Each input port (0 and 1) can receive, and the output port (2) can generate locally, a clock of up to 400 MHz. Input signals are terminated through 50 ohms to -2 V.

The SSE has one user-programmable FPGA (Xilinx Virtex II Pro XC2VP2 for raw serial data, with or without frame synchronization, or XC2VP4 for Reed-Solomon coding).

EDT provides FPGA configuration files — including, for the XC2VP4 FPGA, files for more extensive Reed-Solomon and serial port diagnostics.

Also provided are two user-defined LEDs.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Applications

- Signal receiver and transmitter
- Communications monitoring (serial data)
- Satellite ground station support

Engineering Design Team, Inc. | 3423 NE John Olsen Ave. Hillsboro, Oregon 97124 USA | Tel: +1-503-690-1234 (800-435-4350) | Fax: +1-503-690-1243 | info@edt.com | edt.com

Specifications

Product Type	SSE: Synchronous serial ECL interface; it requires an EDT PCI / PCIe main board.		
FPGAs and Memory	One programmable FPGA (Xilinx Virtex II Pro XC2VP2 or XC2VP4), plus FPGA and memory resources on main board		
Clocks	Port 0 - input		Can receive a clock of up to 300 (Reed-Solomon) or 400 (serial) MHz
	Port 1 - input		Can receive a clock of up to 300 (Reed-Solomon) or 400 (serial) MHz
	Port 2 - output		Can locally generate a clock of up to 300 (Reed-Solomon) or 400 (serial) MHz
Data Rates	Dependent on such factors as data format, main board, and system variables.		
Data Format (I/O)	Three ports are included, supporting the data formats shown below.		
		Termination	**Clock and data each have**
	Port 0 - input	50 ohms to -2 V	One ECL differential pair; serial data can have frame synchronization
	Port 1 - input	50 ohms to -2 V	One ECL differential pair; serial data can have frame synchronization
	Port 2 - output	–	One ECL differential pair; serial data can have frame synchronization
Reed-Solomon Coding	Standard		CCSDS (255,223)
	Frame synchronizer		32-bit pattern and 32-bit mask
	Frames – check and flywheel		Up to 15 of each
Connectors	One 15-pin D		
Cabling	Consult EDT for purchase options.		
Physical	Weight		3.1 oz. typical
	Dimensions		6.6 x 4.2 x 0.75 in. (with a main board)
Environmental	Temperature (operating / non-operating)		0° to 40° C / -40° to 70° C
	Humidity (operating / non-operating)		1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.		

Ordering Options

- Main board: PCI SS / GS or PCIe8 LX / FX / SX
- FPGA: XC2VP2 / XC2VP4

For more options, see main board detail.
Ask about custom options.