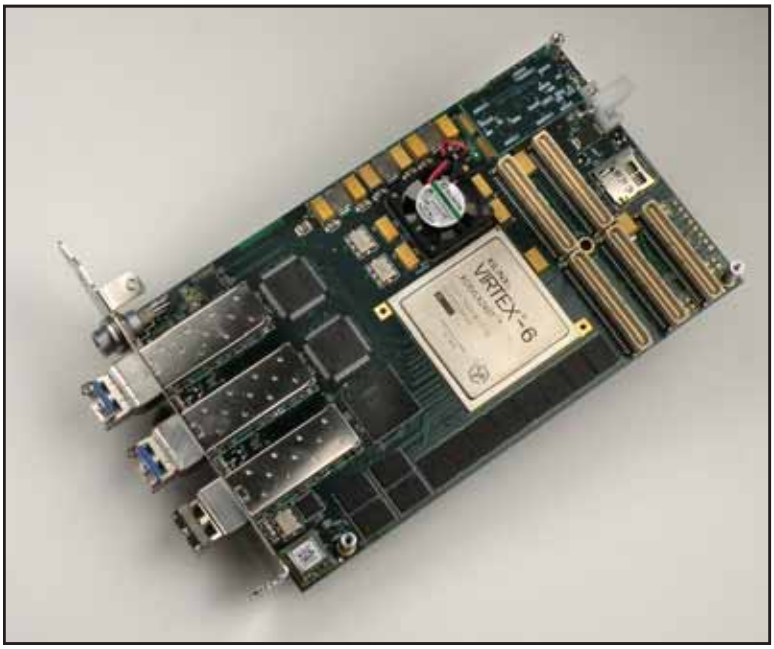
User's Guide

3P

Mezzanine Board



Three-port multirate interface for use with an EDT main board

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Contents

3P Mezzanine Board

Overview

The 3P is a three-port mezzanine board that provides receive-and-transmit capability for these data formats:

- 10GbE (optical only);
- 1GbE (electrical or optical);
- Serial data;
- Optical transport network (OTN); or
- SONET / SDH (OC3 / STM1 through OC192 / STM64).

NOTE In this guide, the signal names SONET (OC3/12/48) and SDH (STM1/4/16) are used interchangeably. For signal standards, see Related Resources on page 11.

Features on the 3P include:

- Three independent blocks of DDR2 DRAM (two can be combined to make a larger block);
- Three programmable oscillators (one per port);
- Three optional small form pluggables (SFP/+ denotes either an SFP or an SFP+) – one per port;
- Three optional SFP/+ line interface units (LIUs)...
  - — Port 0 = 10G LIU (external) or MGT (on the FPGA);
  - — Port 1 = SDH LIU (external) or MGT (on the FPGA);
  - — Port 2 = SDH LIU (external) or MGT (on the FPGA).

Table 1 shows the defaults and options for each port; other options may be available upon request. For details and illustrations, see Board Architecture on page 23.

Table 1. Options by Port – LIU, Signal, Wavelength, and Module (SFP/+)

Port	LIU	Signal*	Wavelength	Module
0	10G	10GbE (10G Base-R), OTN, or OC192 (STM64)	850 / 1310 nm	SFP+
	MGT	1GbE (1000 Base-X or -T) or serial data	Electrical / 850 / 1310 / 1550 nm	SFP
1	SDH	1 GbE (1000 Base-X or -T), OTN, or OC3/12/48 (STM1/4/16)	Electrical / 850 / 1310 / 1550 nm	SFP
	MGT	1GbE (1000 Base-X or -T) or serial data	Electrical / 850 / 1310 / 1550 nm	SFP
2	[Identical to port 1]			

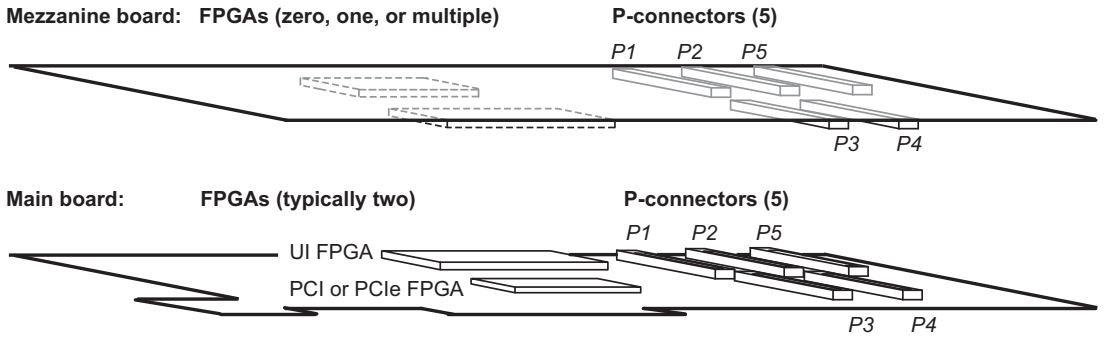
* For details on these standards and parts, see Related Resources on page 11.

The 3P is paired with a PCIe main board for high-speed DMA and other resources. Together, the two boards provide the field-programmable gate arrays (FPGAs) shown below.

FPGAs: Mezzanine Board + Main Board

In general, an EDT board pair can have several FPGAs, as shown in Figure 1.

Figure 1. Generic EDT Board Pair



Not to scale. Generic representations only; actual boards may vary.

In specific, your 3P board pair has the following FPGAs.

- The 3P mezzanine board has one user-programmable FPGA, called the *3P FPGA*. For loading instructions, see Configuring the 3P: Initialization and Setup on page 16.
- The PCIe main board has two FPGAs:
  - The *user interface (UI) FPGA* links the 3P FPGA to the main board's PCI or PCIe FPGA. Loading details are in the PCIe Main Board User's Guide (see Related Resources on page 11).
  - The *PCIe FPGA* communicates with the host computer over the PCIe bus and implements the DMA engine, which transfers data between the board and the host. This FPGA loads automatically, at powerup, with the correct firmware from the main board's FPGA configuration flash memory.

These FPGAs will be discussed in more detail throughout the rest of this guide.

Related Resources

The resources and documentation below may be helpful or necessary for your applications.

EDT Resources

Description	*Detail*	*URL*
• 3P specifications	Datasheet	www.edt.com [find product page]
• PCIe8 LX/SX/FX documentation	Datasheet & user's guide	"
• Time Distribution documentation	User's guide	"
• Application Programming Interface	HTML and PDF	www.edt.com/api
• Installation packages (Windows)	Driver software & firmware downloads	www.edt.com/software.html

Standards

Description	*Pertains to*	*Documentation*	*URL*
• International Telecommunications Union (ITU)	Optical Transport Network (OTN)	G.709/Y.1331 03/2003	www.itu.int
• IEEE	Ethernet framing	IEEE 802-3	www.ieee802.org/3/

Parts

Description	*Part Number*	*Manufacturer*	*URL*
• 3P FPGA - Virtex 6	XC6VLX240T, LX365T, SX315T, or SX47ST	Xilinx	www.xilinx.com
• Line interface units (LIUs) – external:			
– 10G	S19250	Applied Micro	www.appliedmicro.com
– SDH	SLK2511	Texas Instruments	www-s.ti.com/sc/ds/slk2511.pdf
• SFP/+ modules (nm):			
– SFP+ (850)	FTLX8571D3BCL	Finisar	www.finisar.com
– SFP+ (1310 / 1550)	FTLX1371D3BCL	"	"
– SFP (electrical)	FCMJ85213	"	"
– SFP (850)	FTLF8524P2WNV	"	"
– SFP (1310)	FTLF1321P1BTL	"	"
– SFP (1550)	FTLF1521P1BCL	"	"
• Programmable crystal oscillator (XO)	Si570	Silicon Labs	www.silabs.com

Installation and the EDT Installation Package

To physically install the 3P, follow the steps below while referring to Figure 3 on page 23.

1. Power off your system; EDT recommends doing so before removing or replacing any transceiver, despite manufacturers' claims that transceivers are hot-swappable.
2. Using static-dissipative precautions, remove the board pair from its shipping packaging.
3. Make a note of the position of each SFP/+ on the 3P mezzanine board (they can be different, so you'll need to remember which one goes where).
4. Remove the SFP/+s to enable the board pair to fit into the host system.
5. Insert the board pair into the host system.
6. Working through the back panel on the host system, place each SFP/+ back into its original position.
7. Review the EDT installation package resources. as explained in the rest of this section.

NOTE For a link to the latest installation packages, see Related Resources on page 11. For new installations, use the latest package; for existing applications, upgrade only if you have a specific reason to do so.

The PCD Device Driver

Your EDT installation package contains the PCD device driver – the software that runs on the host computer and allows it to communicate with your EDT product. The driver is loaded into the kernel upon installation and runs as a kernel module. The driver name and subdirectory is specific to your operating system, and the installation script automatically installs the correct driver in the correct manner.

Firmware: FPGA Configuration (`.bit`) Files

Included in your EDT installation package, as shown in Table 2 on page 13, are firmware files, also called FPGA configuration (`.bit`) files. Each firmware file is FPGA-specific and interface-specific, so each FPGA must be loaded with the correct one. For the PCIe FPGA, EDT preloads the correct file, which is implemented automatically at system power-on by nonvolatile (flash) memory; however, other FPGAs must be loaded by the user.

For specific details on loading the firmware, see Configuring the 3P: Initialization and Setup on page 16.

NOTE In addition to the firmware files listed in this user's guide, custom firmware files may be requested.

Table 2. Firmware (`.bit`) files

To see firmware for...	...look in this subdirectory...	...for file(s) named...	...loaded in this way...
Main board PCIe FPGA	`flash/`*`FPGApart#`*	[n/a; file is preloaded]	Automatically, by flash
Main board UI FPGA	`bitfiles/`*`FPGApart#`*	`threep.bit`	Manually, by user
Mezzanine board FPGA	`bitfiles/`*`FPGApart#`*	[see list below*]	Manually, by user

* In the mezzanine board subdirectory, you'll find these files...

`threep_10g_sdh_sdh.bit`	If all three ports have SDH LIUs, this file configures the 3P FPGA thus: Port 0 = 10G Base-R Port 1 = OC3/12/48 (STM1/4/16) Port 2 = OC3/12/48 (STM1/4/16)
`threep_10g_emac_emac.bit`	If port 0 has a 10G LIU, and ports 1 and 2 have MGTs, this file configures the 3P FPGA thus: Port 0 = 10G Base-R Port 1 = 1GbE (via MGT) Port 2 = 1GbE (via MGT)
`threep_stm64_sdh_sdh.bit`	If all three ports have SDH LIUs, this file configures the 3P FPGA thus: Port 0 = OC192 (STM64) Port 1 = OC3/12/48 (STM1/4/16) Port 2 = OC3/12/48 (STM1/4/16)
`threep_sdh_sdh_sync.bit`	If ports 1 and 2 have SDH LIUs, this file configures the 3P FPGA thus: Port 0 = not used Port 1 = OC3/12/48 (STM1/4/16) Port 2 = OC3/12/48 (STM1/4/16)

Applications and Utilities

In addition to the above resources, the EDT installation package includes application and utility files that you can use to initialize and configure the board, access the registers, and perform basic self-testing. In many cases, C or C++ source is provided so you can use the files as starting points to write your own applications. The most commonly useful files are described below; for a complete list, see the README file.

These 3P files are in the top-level directory of your EDT installation package...

`lib_threep.c`	C library routines that you can use in your 3P applications.
`edt_threep.h`	Include file for the above C library routines.
`threep_setup`	Utility application that configures the LIU on port 0 and sets up each port's reference clock.
`threep_setup.c`	C source for `threep_setup`.

In addition, the 3P is supported by C++ files in the subdirectory `libocx`. The below resources are in the C++ library at `libocx.lib` (for Windows) or `libocx.so` (for Linux).

`OCXSnap`	Example application that captures data from the 3P board and transfers it to disk for testing or verification.
`OCXSnap.cpp`	C++ source for `OCXSnap`.
`OCXPlay`	Example application that outputs the data captured by `OCXSnap` from the disk for testing or verification.
`OCXPlay.cpp`	C++ source for `OCXPlay`.

`ReadXFPSFP`	Example application that queries the state of the transceiver modules. For details, see Initializing and Enabling the Data Paths on page 20.
`ReadXFPSFP.cpp`	C++ source for `ReadXFPSFP.`

Sample Applications

`simple_getdata`	Serves as an example of a variety of DMA-related operations, including reading the data from the connector interface and writing it to a file, as well as measuring input rate.
`simple_putdata`	Serves as an example of a variety of DMA-related operations, including reading data from a file and writing it out to the connector interface.
`test_timeout`	Under normal operation, timeouts cancel DMA transfers. This application exemplifies giving notification when a timeout occurs, without canceling DMA.

Utilities

`pdb`	Enables interactive reading and writing of the UI FPGA registers.
`timing_test`	Programs the timecode microcontroller and tests the timecode input.

Basic Testing

Various files (source, executables, and FPGA configuration files) are available to help you perform basic testing on your EDT board (see Basic Self-Testing on page 22). These files include at least...

`sslooptest`	Verifies installation and basic functioning of most EDT PCIe boards. Determines board model and runs appropriate loopback test.

Building or Rebuilding an Application

In your EDT installation package, executable and PCD source files are in the top-level directory. Therefore, if you need to build or rebuild an application, run `make` in that directory.

Windows users must install a C compiler; EDT recommends the Microsoft Visual C compiler for Windows. Linux users can use the `gcc` compiler typically included with the Linux installation.

After you build or rebuild an application, use the `--help` command-line option for a list of usage options and descriptions.

OCXSnap and OCXPlay

With their source code, the two command-line applications `OCXSnap` and `OCMPlay` provide an example of capturing data and playing it back. They can be invoked with various options for customization.

NOTE C software on earlier EDT boards (e.g., OCM, OC192) invoked programs via DMA channel, with each DMA channel linked to a specific DMA direction and physical port on the board; however, the new `libocx` library uses an argument to specify which port. This change was needed because the 3P uses four DMA channels but has six possible port / direction combinations.

If possible, the software will use the specified clock speed to select the correct channel.

If not, you can specify which port by entering...

`-P` *`port#`*

...replacing *`port#`* with the desired port number.

For a Help message listing all usage options, invoke these applications with the flag `-h`. For example...

```
OCXSnap -h
```

The following example captures 2048 MB (2GB) of an OC3 / STM1 signal from port 1 `(-P 1)` by specifying a line rate of 1 `(-r 1)` for OC3 / STM1 and an output file size of 2048 MB `(-s 2048)`...

```
OCXSnap -P 1 -r 1 -s 2048 -o outputfilename
```

...where 1 represents the numeric digit “1” and *`outputfilename`* represents the name of the output file.

After about two minutes, when the application terminates, the companion invocation of `OCXPlay` outputs the captured data from port 1 at the OC3 / STM1 line rate, with input from the specified file...

```
OCXPlay -P 1 -r 1 -i inputfilename
```

...where 1 represents the numeric digit “1” and *`inputfilename`* represents the name of the input file.

The above example requires a host disk system that can read and write a file at 20 MB per second; the comparable run for OC12 / STM4 data requires a disk system that can function at 80 MB per second.

Below are a few considerations not provided in the Help message...

- The example application `OCXSnap` allows you to specify that the output be formatted in hexadecimal chunks of 32, 16, or 8 bits, using the flags `-H`, `-Hw`, or `-HHb`, respectively. In all cases, the most significant bit is the first bit output (in time) and the leftmost bit of the chunk (in memory).
- The flag `-s` to `OCXSnap` specifies the final file size in megabytes. The application will terminate when the specified size has been reached.
- The application `OCXSnap` allows you to change the default number and size of the ring buffers using the flags `-n` and `-b`. For performance reasons, the ring buffer size is always rounded to the nearest multiple of 4096. The application then checks to determine whether the requested size and number of ring buffers is reasonable for the line rate. if it is not, the application configures the ring buffers as requested, but emits a warning message.
- Both `OCXSnap` and `OCXPlay` are designed to run basic initialization by default. If you want to skip basic initialization (for example, if another program has already performed it and you do not want to run it again), you can do so by using the `-I` initialization flag.

Configuring the 3P: Initialization and Setup

In the `libocx` library, the EDT board and its configuration are treated as two distinct entities: The board is an object derived from an abstract base class `EdtOCX`, while the configuration is an object of class `EdtOCXCfg`. The `config` class has built-in argument parsing to set its various options.

The example applications initialize the 3P by synchronizing the digital PLLs that produce the clock signals, initializing the port 0 memory (if any), enabling the LIUs, and enabling the data paths. If you are using the EDT example applications, this initialization happens automatically. If, however, you are writing your own application for the 3P, you will need to use the correct initialization sequence.

Initializing the Board and Preparing for DMA

To open the board class derived from `EdtOCX` you'll need to set up the configuration object. To do so, set up the member variables of this object in a command-line–based program by passing in to the `EdtOCX::ParseOptions` function the `argc` and `argv` arguments passed into your `main()` function

The example below shows a way to create the `EdtOCXCfg` configuration object and parse arguments. The routine `cfg.Init()` sets the default flags and data rate for this program, all of which will be overwritten by options parsed by the routine `cfg.ParseOptions()`.

```
EdtOCXCfg cfg;
EdtOCX *board;
```

Figure A. To set the default flags, the timeout in milliseconds, and the default line rate, enter...

```
cfg.Init(
   EDT_OCX_FULL_INIT | EDT_OCX|FRAMED | EDT_OCX_ENABLE_MEM | EDT_OCX_sWAP, 1000,
   STM16_RATE);
   cfg.ParseOptions(argc, argv, true);
```

After the configuration is set, it can be used to open the correct mezzanine board...

```
board = EdtOCX::OpenBoard(&cfg, false);
```

Now the board can be initialized based on the values in the `EdtOCXCfg` object.

For complete initialization, which will allow DMA to be enabled, run...

```
rc = Board->Configure(); // The value returned will be 0 for success, or -1 for failure.
   // The Configure function will load the appropriate FPGA configuration files, set up
   // the clocks, and synchronize with the input signal.

Board->SetupDma(); // This uses default values for buffer size based on effective data
   // rate.
```

To verify the state of the signal after initialization, run...

```
Board->HasSignal();
Board->IsFramed();
```

To start DMA, run...

```
Board->ChannelStart(); // This will initiate the DMA.
```

Configuring the FPGAs

EDT FPGA configuration includes some steps that are automatic, and some that must or may be done manually. The procedures in this section cover both automatic and manual (direct) board setup.

Unit number

The first step in setting up each board pair is to determine its system-assigned unit number (by default, 0).

To do so, run...

```
pciload
```

...with no arguments, and the screen will display information about each unit.

Main board PCIe FPGA

The main board PCIe FPGA is configured automatically at power-on via flash memory. This FPGA generally does not need to be reconfigured or updated unless...

- you are asked to do so by EDT during a support call or email exchange; or
- you install a new driver.

To verify the loading of the correct main board PCIe FPGA configuration file (`pe8lx4.bit` or `pe8lx16.bit`):

1. Navigate to the directory in which you installed the driver. The default location is `\EDT\pcd` in Windows.
2. At the prompt, enter...

   ```
   pciload verify
   ```

   ...to compare the PCIe FPGA configuration file in the installation package with the one already loaded in flash memory. If multiple boards are installed, enter...

   ```
   pciload -u unit# verify
   ```

   ...replacing *`unit#`* with the unit number.

   If the dates and revision numbers match, there is no need to upgrade. If they differ, you can proceed through the steps below to upgrade the flash memory.
3. At the prompt, enter...

   ```
   pciload update
   ```
4. Power-cycle the host computer (power off, then on – a simple reboot is not enough) to implement the new FPGA configuration file.

Main board UI FPGA and mezzanine board 3P FPGA

The main board UI FPGA is configured automatically when you manually load the mezzanine board 3P FPGA. If necessary, you can set up the 3P directly by reading and writing the onboard registers; however, to do so, you must manually load the UI FPGA before loading the 3P FPGA.

To set up the board with either the automatic or the manual (direct) setup option...

1. For automatic setup of the UI FPGA and the mezzanine board 3P FPGA, skip to the next step.

   For manual (direct) setup of the UI FPGA, run the *`bitload`* utility...

   ```
   bitload -u unit# threep
   ```

   ...replacing *`unit#`* with the unit number.
2. Next, to set up the 3P FPGA, run the *`mezzload`* utility...

   ```
   mezzload -u unit#
   ```

   ...replacing *`unit#`* with the unit number.

   If you do not specify an FPGA configuration file, then *`mezzload`* will load the following file...

   ```
   threep_stm64_sdh_sdh.bit
   ```

If you do wish to specify an FPGA configuration file, then enter...

```
mezzload -u unit# FPGAconfigurationfilename
```

...replacing *unit#* and *FPGAconfigurationfilename* with the appropriate information.

Initializing the Clock Signals and Logic Circuits

This procedure initializes basic board operations, as well as communication between the main board's UI FPGA and the mezzanine board's 3P FPGA. Such communication is synchronized to the 100 MHz reference clock signal, which is initialized automatically upon main board startup but then must be distributed to the 3P FPGA. Until the 3P FPGA is synchronized to the reference clock signal, the main board cannot read or write any registers on the 3P mezzanine board (which reside in the range from 0x80 to 0xFF).

The `EDTOCX` member function `board->BaseInit()` determines the kind of board installed in your system, loads the main and mezzanine FPGA configuration files if needed, and performs the steps below. It uses an `EDTOCXCfg` structure to set bits 0 and 3 (SSWAP and BSWAP) in 0x0F Configuration as needed for your host, as well as to set other fields. For details on filling in the fields in this structure, consult the EDT API documentation (see Related Resources on page 11); for an example of its use, see the example application `OCXSnap.cpp`.

The routine `board->BaseInit()` typically is used to initialize clock signals and logic circuits.

To do so...

1. Load the appropriate firmware as described in Configuring the 3P: Initialization and Setup on page 16. The firmware will perform various actions, including initializing the main board PLL that generates the 100 MHz reference clock.

NOTE If the firmware is loaded already and you do not wish to reload it, clear 0x00–7F [See threep.bit] and then clear the appropriate enable registers (0x83–84 for port 0, 0xA3–A4-for port 1, 0xC3–C4 for port 2) by writing all zeroes.

2. To initialize the logic circuits in the UI FPGA on the main board, set bit 3 (CMD_EN) in 0x00–7F [See threep.bit].
3. To ensure that the FPGAs on the 3P mezzanine board have been synchronized, verify that bit 5 (SYS_LOCK) of 0x84 Port 0 Enable is set.
4. To ensure that the main board's UI FPGA has been synchronized, verify that bit 0 (LOCAL_SYS_LOCK) of 0x06 PLL Status is set.
5. At this point, insert a timeout in your application (the library routine `edt_ocx_base_init` does so). The bits in steps 3 and 4 should be set within approximately 10 milliseconds of the bits in steps 2 and 3; if they are not, there is probably a fault in the board. In such a case, without a timeout your application will hang; inserting a timeout of approximately half a second should resolve the issue.
6. If the bits in steps 3 and 4 still are not set, stop initialization and contact EDT.

The main board is now set up correctly; basic initialization is complete and does not need to be done again until the host computer is power-cycled.

Initializing the Memory

After the system PLL is synchronized, you'll need to initialize the memory blocks on your 3P.

To do so...

1. Clear bit 0 (PHY_RST) in 0xE4–E6 DDR2 Bank Status and Control.
2. Include a timeout for the RAM to finish initialization and for the refresh to stabilize – for example:

   ```
   edt_msleep(10)
   ```

3. Wait for bits 5 and 6 (PLL_LOCK and PHY_INITDONE) in 0xE4–E6 DDR2 Bank Status and Control to be set.

The memory now is available for use. This operation, too, need not be repeated until you restart your application.

Enabling and Verifying the Input Signals – Ports 1 and 2

Each port has two digital phase-locked loops (PLLs) — one for the LIU and one for the FPGA — which must be locked to the incoming data. If the data is interrupted or not present, these PLLs must be reset. The data paths can be initialized independently, so you can perform this procedure for one port or DMA channel even if another is acquiring data.

To do so, follow the steps below.

1. Prepare a channel to acquire data by using the library routines...

   ```
   board->PortSetRate()
   port->IoPortSetup()
   ```

2. Lock the PLLs by using the library routine...

   ```
   board->LockFrontend()
   ```

Except where noted, `board->LockFrontend()` performs the procedure below.

1. Clear bits 0 (LIU_EN), 1 (TPLL_EN), and 4 (RPLL_EN) in the desired register (0x84 Port 0 Enable).
2. To enable the LIU, set bit 0 (SLK_EN) bit in the desired register (0x84 Port 0 Enable).
3. Wait approximately 100 milliseconds.
4. Verify that the SFP transceiver module has detected an incoming signal by checking bit 7 (SIG_DET) in the desired register (0xA2 Port 1 Status).
5. Loop until bit 7 (SIG_DET) is set, showing application status as necessary.
6. To ensure that the LIU PLL is locked, verify that bit 4 (LOL) in the desired register (0xA2 Port 1 Status) is clear; if it is set, the LIU is not receiving a stable input signal in the range of the selected reference clock. In certain cases, the LOL bit can be clear even if the PLL is not locked. If the phase difference between the incoming data and the reference clock differs by more than 500 parts per million, the LOL state is not valid (for details on the SDH LIU, see Related Resources on page 11).
7. For incoming framed SONET / SDH signals, you may wish to verify that bit 5 (LOS) in the desired register (0xA2 Port 1 Status) is clear; if it is set, the LIU is not receiving a framed SONET / SDH signal. (Bit 5 can be clear only for framed SONET / SDH signals and is meaningless for other signals.) This step is not performed by `board->LockFrontend()`.
8. To enable the PLLs in the FPGA that communicates with the LIU: Set bits 1 (TPLL_EN) and 4 (RPLL_EN) in the desired register (0x84 Port 0 Enable).
9. To verify that the receive clock PLL is locked to the receive clock of the LIU, verify that bits 6 and 7 (THREEP_RX_LOCKED and THREEP_TX_LOCKED) of the desired register (0x84 Port 0 Enable) are set. If they are clear, the board is not receiving an input signal, so you'll need to restart the data path initialization procedure from the beginning.

NOTE Your code can implement steps 1 through 9 as a loop.

10. If you are receiving a framed SONET/SDH signal, you can verify that it is properly framed and gather statistics about the quality of signal framing. Bit 7 (LOCKED) in 0xA8 Port 1 Receive Frame Status tells you if the signal is currently in frame.The library routine `board->EnableFramingErrors` enables the error counter registers, which track how many errors have occurred in signal framing and what types of errors they are. This routine sets bit 7 (EN_COUNTERS) in 0x8B Port 0 Frame Statistics Count Control. The framing error registers are:
    - 0xA8 Port 1 Receive Frame Status;
    - 0x800105–07 Port 1 B1 Error Count;
    - 0x800108–0B Port 1 B2 Error Count;
    - 0x80010C–0E Port 1 M1 Error Count;
    - 0x80010F–10 Port 1 Loss of Frame Count;
    - 0x800111–12 Port 1 Frame Pattern Error Count.

The library routine `board->EnableFramingErrors` accesses these registers and returns the information by filling in the structure `EdtOCXFrameErrors` defined in `edt_ocx.h`.

Initializing and Enabling the Data Paths

To initialize and enable the data paths...

1. Configure DMA as required, using the library routine `board->SetupDma()`.
2. Set up and enable each port / DMA channel using the C++ library routine `board->ChannelStart()`.
3. Start DMA using the library routine `edt_start_ring_buffers`.
4. Your application can now start transmitting or receiving data by setting the appropriate bits (0–3, CH_ENABLE) in 0x10–11 DMA Channel Enable, or by calling the library function `board->SetChannelEnable()`.

Querying the SFP/+ Transceivers

Each SFP/+ transceiver has a two-wire serial interface that lets you query its state, including:

- The laser's transmit power, in decibels;
- The laser's receive power, in decibels; and
- The temperature of the SFP/+ in degrees Celsius.

For details, see the manufacturer's product information for the SFP/+ you are using (see Related Resources on page 11).

By default, each SFP/+ is enabled.

The application `ReadXFPSFP` will let you query and control each SFP/+ via the two-wire serial interface.

- To enable the SFP/+ via the two-wire serial interface, enter...

  ```
  ReadXFPSFP -e 1
  ```

- To disable the SFP/+ via the two-wire serial interface, enter...

  ```
  ReadXFPSFP -e 0
  ```

- To turn on the laser after the SFP/+ is enabled, enter...

  ```
  ReadXFPSFP -l 1
  ```

- To turn off the laser while keeping the SFP/+ enabled, enter...

  ```
  ReadXFPSFP -l 0
  ```

Time Code

The 3P uses the same timecode interface as the EDT Time Distribution board. For details, see registers 0xEB–ED Time Distribution and the Time Distribution user's guide (Related Resources on page 11).

Framing

The 3P supports framing capability for OTN, OC / STM, and 10GbE, as described below.

OTN and OC / STM

For OTN and OC / STM, framing headers are included in the data transferred during DMA. If framing is enabled, the board searches and locks onto incoming SONET / SDH frames after detecting the presence of A1 and A2 header patterns at 125-millisecond intervals. The algorithm sequence is...

1. Search. The board searches for A1 and A2 header patterns until it sees a match; then it goes to Check.
2. Check. The board checks for three consecutive SONET / SDH frames at 125-microsecond intervals with the A1 and A2 header patterns in the proper position, before declaring Lock.
3. Lock. Once locked, incoming SONET / SDH frames are collected and forwarded to the host. The board continues to check for the A1 and A2 header patterns, and remains in this state until the A1 and A2 header patterns are lost. When the patterns are lost, it enters the Flywheel state.
4. Flywheel. If the A1 and A2 header patterns are not seen for three consecutive frames, the board returns to Search; if it finds them, it returns to Lock. SONET / SDH frames are collected and forwarded to the host in this state as well.

10 GbE

For 10 GbE, framing information is provided in such registers as...

- 0x85 Port 0 Receive Framing Control;
- 0x86 Port 0 Receive Filter Control;
- 0x8E Port 0 PCS Control.

For details, contact EDT (tech@edt.com).

Basic Self-Testing

The loopback test determines the board configuration, loads the appropriate FPGA configuration file, generates test data, and tests the board and its components with no external device connected. For included test files, see Basic Testing on page 14 (under Sample Applications).

NOTE The loopback test overwrites the FPGA configuration file in the UI FPGA. After completing the test, you must reconfigure the board before using it again.

To perform the loopback test:

1. Keep the board in the host computer with the mezzanine board (if any) attached, but disconnect any external device and its cabling.
2. In a command window, enter...

   `sslooptest -u` *`unit number`*

   The outcome varies depending on your main-mezzanine board pair. Errors are directed to the file `sslooptest.err` in the current directory; if no such file exists, the test completed without errors.

Loopback test output for a functional board contains such lines as:

```
Total errs=0 bufs=4000; Channel errs(NNNNxxxxxxxxxxxx) bufs(YYYYxxxxxxxxxxxx)
```

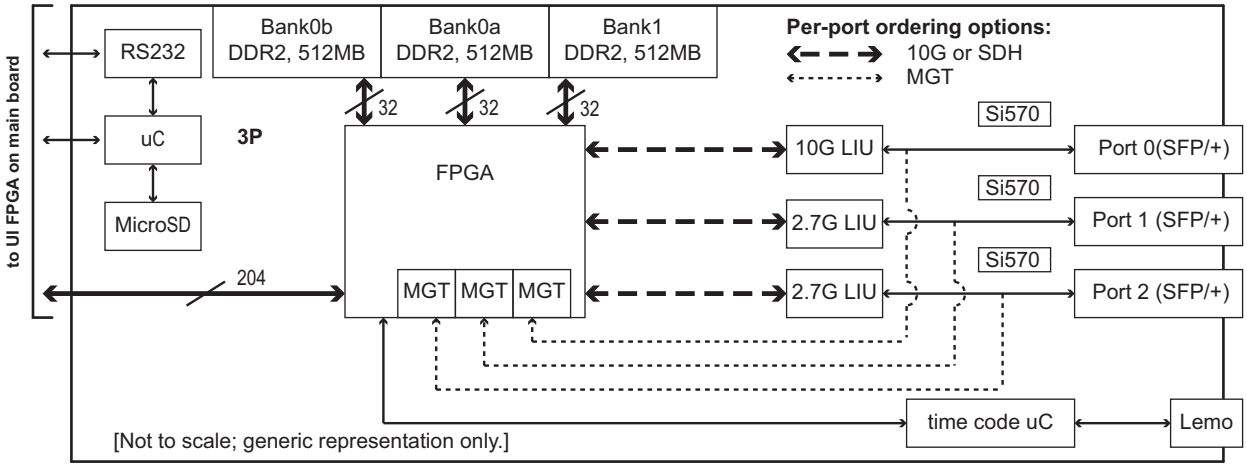
- The value after `Total errs` shows the error count so far.
- The value after `bufs` shows the number of buffers in use.
- The characters after `Channel errs` correspond to DMA channels 0-15 (in that order). For each DMA channel, `Y` means a data error, `N` means no data error, and `X` means that channel is not in use.
- The characters after `Channel... bufs` also correspond to DMA channels 0-15. For each DMA channel, `Y` means the buffer is in use, `N` means no DMA is occurring, and `X` means that channel is not in use.

3. After the test is done, reconfigure the board with `initpcd` (or your own application) to disable loopback.
4. Reconnect the board to the external device.

Board Architecture

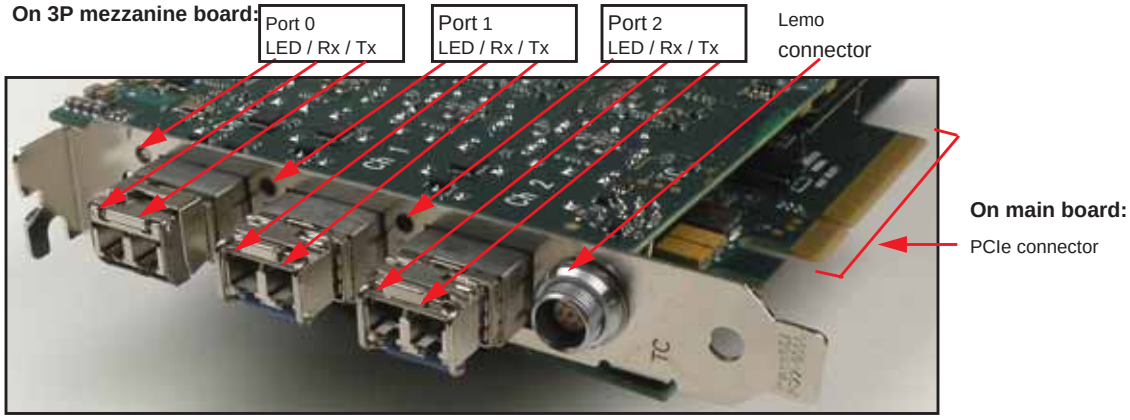
The 3P mezzanine board works with an EDT main board. Figure 2 shows various features on the 3P alone, while Figure 3 shows the 3P with a main board and indicates the location of the connectors and LEDs.

Figure 2. Block diagram – 3P mezzanine board



NOTES: Banks 0b and 0a can be combined as a 64-bit-wide 1GB memory bank.
Si570 oscillators are programmable via I2C and provide reference clocks directly to LIUs and MGTs.

Figure 3. 3P mezzanine with main board, showing connectors and LED status indicators



The 3P mezzanine board (on top) shows the SFP/+ transceivers with their port connections, and the Lemo connector for timecode input. The main board (on the bottom) shows the location of the PCIe connector.

NOTE The 3P ports are labeled on the front panel as follows: “Ch 0” (port 0) is the SFP/+ furthest from the PCIe connector; “Ch 2” (port 2) is the SFP/+ nearest the PCIe connector.

Each port has one bicolor LED (controlled by the 3P FPGA) to indicate the status of that port in three areas:

- Is the FPGA receive clock locked?
- Is a signal being received?
- Is the signal being framed?

If a port is working properly in all three areas, its LED will be green. If a port has problems with receiving and framing a signal, its LED will be red. If a port has a combination of red and green conditions, the two colors will combine to make a third color, which is orange.

If you are using an EDT FPGA configuration (`.bit`) file, during board initialization each port's LED initially will blink red or orange, and then will change to steady red, orange, or green.

Table 3 summarizes these LED behaviors.

Table 3. LED behaviors generated by EDT FPGA configuration (`.bit`) files

LED behavior	Clock locked?	Signal received?	Signal framed?
Blinking red	No	No	No
Blinking orange	No	Yes	No
Steady red	Yes	No	No
Steady orange	Yes	Yes	No
Steady green	Yes	Yes	Yes

APPENDIX A: Main Board UI FPGA Configuration File

Overview

This appendix documents the registers for the following main board UI FPGA configuration files, as found in your EDT installation package.

`threep.bit`	For the main board UI FPGA (on the PCIe8 LX/FX/SX main board).

threep.bit

0x00–0x7F Main Board

0x00 Command

		Access / Notes	8-bit read-write / PCD_CMD
Bit	**Access**	**Name**	**Description**
7–4	–	PCD_STAT_INT_EN	Enables interrupts as defined in registers 0x03 Interrupt Status and 0x04 Interrupt Enable.
3	RW	CMD_EN	Set this bit and enable the required DMA channels in 0x10–11 DMA Channel Enable for DMA. When clear, resets all DMA channels, flushes all FIFOs, and clears all under- and overflow bits.
2–0	–	[no name]	Reserved.

0x03 Interrupt Status

		Access / Notes	8-bit read-only / PCD_STAT
			This register is connected to 1Hz test interrupt as an example of interrupts generated by the UI FPGA on the main board.
Bit	**Access**	**Name**	**Description**
7–4	R only	PCD_STAT_INT	Interrupt bits for the status bits. If the corresponding bit is asserted in 0x00 Command, then the corresponding bit of these four can be asserted to cause a PCI bus interrupt. The PCI bus interrupt then is caused when the corresponding PCD_STAT signal [bits 3–0] is asserted. To reset the interrupt, disable and re-enable the appropriate PCD_STAT_INT_EN bit [7–4] in 0x00 Command.
3–0	R only	PCD_STAT	The state of user-definable STAT input signals as last sampled.

0x04 Interrupt Enable

		Access / Notes	8-bit read-write / PCD_STAT_POLARITY
			This register is connected to 1Hz test interrupt as an example of interrupts generated by the UI FPGA on the main board.
Bit	**Access**	**Name**	**Description**
7–5	–	[no name]	Reserved.
4	RW	PCD_STAT_INT_ENA	Provides global enable or disable for all interrupt bits [7–4] in 0x03 Interrupt Status above, allowing the driver to disable and re-enable them in one operation without altering their states. A value of 1 enables the interrupts; a value of 0 disables them.
3–0	–	[no name]	Reserved.

0x05 FPGA Configuration File Organization

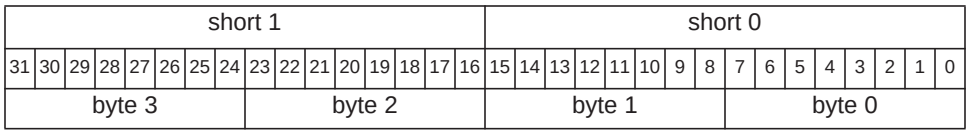
		Access / Notes	8-bit read-only / PCD_ORG
Bit	**Access**	**Name**	**Description**
7–0	R only	[no name]	Specifies the organization that created the FPGA configuration file currently loaded in the UI FPGA on the main board. An EDT FPGA configuration file returns the value 0xFF.

0x06 PLL Status

		Access / Notes	8-bit read-only / [no name]
Bit	**Access**	**Name**	**Description**
7–1	–	[no name]	Reserved.
1	R only	[no name]	If set, the 100 MHz clock used for data transfers from the mezzanine to the main board is locked.
0	R only	LOCAL_SYS_LOCK	If set, the 100 MHz reference clock is locked.

0x0F Configuration

		Access / Notes	8-bit read-write / PCD_CONFIG
			This register and register 0x16 both can affect how data is ordered.
Bit	**Access**	**Name**	**Description**
7–4	–	[no name]	Reserved.
3	RW	SSWAP	Short swap bit; swaps the two 16-bit short words in one 32-bit data word, so that *short 1*is transferred before *short 0*. Does not change the order of the bits within each short.
2–1	–	[no name]	Reserved.
0	RW	BSWAP	Byte swap bit; swaps bytes 0 and 1, and also bytes 2and 3, in a 32-bit data word, so that the bytes are positioned 1, 0, 3, 2. Does not change the position of the bits within each byte. Below is the structure of a 32-bit data word, with no swapping in effect. With bit 3 set, short 0 appears before short 1. With bit 0 set, byte 2 is before byte 3, and byte 0 before byte 1. With both set, the order of the bytes is 3, 2, 1, 0.



0x10–11 DMA Channel Enable

		Access / Notes	16-bit read-write / SSD16_CHEN
Bit	**Access**	**Name**	**Description**
15–6	–	[no name]	Reserved.
5–0	RW	CH_ENABLE[5–0]	Set or clear the appropriate bit to enable or reset the corresponding DMA channel: - Set bit 5 to enable transmit data for port 2; clear to reset. - Set bit 4 to enable transmit data for port 1; clear to reset. - Set bit 3 to enable transmit data for port 0; clear to reset. - Set bit 2 to enable receive data from port 2; clear to reset. - Set bit 1 to enable receive data from port 1; clear to reset. - Set bit 0 to enable receive data from port 0; clear to reset.

0x12–13 DMA Channel Direction [Reserved]

0x14–15 DMA Channel Edge [Reserved]

0x16 Least Significant Bit First

		Access / Notes	16-bit read-write / SSD16_LSB
			This register and 0x0F Configuration both can affect the order of bits in a 32-bit word.
Bit	**Access**	**Name**	**Description**
7–6	–	[no name]	Reserved.
5–0	RW	LSB_FIRST[5–0]	When set for a DMA channel, the least significant bit of the 32-bit data word is first, and the most significant bit is last; when clear, the most significant bit of a 32-bit word is first.

0x18–19 Underflow

		Access / Notes	8-bit read-only / SSD16_UNDER
Bit	**Access**	**Name**	**Description**
15–6	–	[no name]	Reserved.
5–0	R only	UNDERFLOW[5 –0]	A value of 1 in a bit indicates that the corresponding DMA channel's internal FIFO has underflowed since the channel was last enabled. Underflow causes the corresponding DMA channel to transmit the last valid byte repeatedly until it receives new DMA data. To reset, clear and reenable the appropriate channel (see 0x00 Command and 0x10–11 DMA Channel Enable).

0x1A–1B Overflow

		Access / Notes	16-bit read-only / SSD16_OVER
Bit	**Access**	**Name**	**Description**
15–6	–	[no name]	Reserved.
5–0	R only	OVERFLOW[5–0]	A value of 1 in a bit indicates that the corresponding DMA channel's internal FIFO has overflowed since the channel was last enabled. Data received while the FIFO is in overflow is discarded. To reset, clear and reenable the appropriate channel (see 0x00 Command and 0x10–11 DMA Channel Enable).

0x40–43 Mezzload

		Access / Notes	32-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
31–0	RW	[no name]	Reserved. Do not write this register space; it is used by `mezzload` to configure the 3P FPGA (on the 3P mezzanine board).

0x44 Mezzload Control / Select

		Access / Notes	8-bit read-write / [no access name]
Bit	**Access**	**Name**	**Description**
7–1	–	[no name]	Reserved.
0	RW	[no name]	Reserved. Do not write this register space; it is used by `mezzload` to configure the 3P FPGA (on the 3P mezzanine board).

0x4A Port 2 DMA Transmit Mode

		Access / Notes	8-bit read-write / [no name]
			Enables special modes for DMA output on port 2. For details, see Initializing and Enabling the Data Paths on page 20.
Bit	**Access**	**Name**	**Description**
7–3	–	[no name]	Reserved.
2	RW	[no name]	Set to force DMA channel 3 to output on port 2 (instead of 0).
1–0	RW	[no name]	00 = DMA channel 4 to output on port 1. 11 = DMA channel 5 to output on port 2.

0x60–62 Extended Indirect Register Address

		Access / Notes	24-bit read-write / [no name]
			0x60 = least significant 8 bits; 0x61 = middle 8 bits; 0x62 = most significant 8 bits
Bit	**Access**	**Name**	**Description**
23–0	RW	[no name]	This is the register address space for the extended indirect registers.

0x63 Extended Indirect Register Data

		Access / Notes	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	This is the register data for the extended indirect registers. – Writing this register writes data to the register addressed by 0x60–62. – Reading this register reads the data addressed by 0x60–62.

0x65 Serial Master Interface Status

		Access / Notes	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7	R only	SER_DEV_BSY	Read only. When set, the serial master is busy.
6	R only	SER_DEV_ACK_FAIL	Read only. When set, the serial slave failed to respond to the last command.
5–0	RW	SER_DEV_ADDR	Device 0 = mezzanine microcontroller. Device 1 = reserved. Device 2 = ADT7461 temperature monitor (write interface). Device 3 = ADT7461 temperature monitor (read interface).

0x66 Serial Master Interface Read [7–0]

		Access / Notes	8-bit read-write / [no name]
			Works with 0x69 Serial Master Interface Read [15–8] on page 31 for 16-bit accesses.
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the data returned from address.

0x67 Serial Master Interface Register Address

		Access / Notes	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the previously accessed serial slave register address.

0x68 Serial Master Interface Write

		Access / Notes	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Write data to the register address in register 0x67.

0x69 Serial Master Interface Read [15–8]

		Access / Notes	8-bit read-write / [no name]
			Works with 0x66 Serial Master Interface Read [7–0] for 16-bit accesses.
Bit	**Access**	**Name**	**Description**
15–8	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the data returned from address.

0x7C–7D FPGA Configuration File Design ID

		Access / Notes	16-bit read-only / PCD_DESIGN_ID
Bit	**Access**	**Name**	**Description**
15–0	R only	[no name]	A 16-bit number assigned by the organization that produced the FPGA configuration file loaded in the main board UI FPGA. (EDT uses the top eight bits only.) The design ID for `threep.bit` is 0x1200.

0x7E FPGA Configuration File Version String

		Access / Notes	8-bit read-write / MAIN_BITFILE_VERSION
			To read the FPGA configuration file version string from ROM, write the ROM address to the register and read the ASCII data from the same register. The version string is a maximum of 64 bytes long, so only the first six bits of the address are significant.
Bit	**Access**	**Name**	**Description**
7–0	RW	ID_ADD_DATA	Write an address to read ROM contents. Result is... *mainBoard_mezzBoard_bitfileName version.revision mm/dd/yyyy (number of DMA channels used, number of DMA channels required by PCI FPGA)* *mm/dd/yyyy* is the date the FPGA configuration file was created. Italicized terms are replaced by actual values — for example, `lx16_threep_threep 1.0 08/29/2010 (6,6).`

0x7F Board ID

Access / Notes: 8-bit read-write / EDT_BOARDID

Used to identify EDT mezzanine boards. A value of 0x2 in the lowest four bits indicates an extended board ID, hard-wired into a nonvolatile complex programmable logic device (CPLD). The `extbdid` application seeks the identifier in the board ID register; if it finds a value of 0x2, then it seeks the extended board ID from the CPLD instead.

Bit	Access	Name	Description
7–4	RW	[no name]	Used by `extbdid.exe`.
3–0	R only	BOARD_ID	See the table below for details on EDT board ID and extended board ID (CPLD).

Table 4. EDT Board ID and Extended Board ID (CPLD)

Bd ID Register, Bits 3–0	Ext. Bd ID	Mezzanine Board	* Main Boards It Works With	Detail
0 0 0 0 0x0	–	RS422	LX, GS, SS	–
0 0 0 1 0x1	–	LVDS	LX, GS, SS	–
0 0 1 0 0x2	–	Reserved	–	For extended board IDs (below).
– – – – –	0x0A	SRXL	LX, GS, SS	–
– – – – –	0x10	16TE3	LX, GS, SS	–
– – – – –	0x11	OC192	LX, GS	–
– – – – –	0x12	3x3G	LX, GS, SS	–
– – – – –	0x13	MSDV	LX, GS, SS	–
– – – – –	0x14	SRXL2 (rev01 & 02)	LX, GS, SS	Contact EDT to exchange for later revision.
– – – – –	0x15	Net10G	LX, GS	–
– – – – –	0x16	DRX	AMC	–
– – – – –	0x17	DDSP	LX, GS, SS	–
– – – – –	0x18	SRXL2 (rev03+)	LX, GS	For the IDM + LBM option.
– – – – –	0x19	SRXL2 (rev03+)	LX, GS	For the IDM + IDM option.
– – – – –	0x1A	SRXL2 (rev03+)	LX, GS	For the IMM + IMM option.
– – – – –	0x1B	SRXL2 (rev03+)	LX, GS	For the IMM + LBM option.
– – – – –	0x1C	SRXL2 (rev03+)	LX, GS	For the IDM + IMM option.
– – – – –	0x1D	DRX16	LX, GS	For the IDX + IDX option.
– – – – –	0x1E	OCM2.7G	AMC	–
– – – – –	0x1F	3P	LX	–
0 0 1 1 0x3	–	Reserved	–	–
0 1 0 0 0x4	–	SSE	LX, GS, SS	–
0 1 0 1 0x5	–	HRC	LX, GS, SS	For E4, STS3, STM1 / OC3 I/O.
0 1 1 0 0x6	–	OCM	LX, GS, SS	–
0 1 1 1 0x7	–	Combo 2	LX, GS, SS	For LVDS I/O.
1 0 0 0 0x8	–	ECL/LVDS-E/RS422-E	LX, GS, SS	For ECL, LVDS, RS422, E1/T1 I/O.
1 0 0 1 0x9	–	TLK1501	[Legacy]	–
1 0 1 0 0xA	–	Reserved	–	–
1 0 1 1 0xB	–	Combo 3	LX, GS, SS	For RS422 I/O.
1 1 0 0 0xC	–	Combo 3	LX, GS, SS	For LVDS I/O.
1 1 0 1 0xD	–	Combo 3	LX, GS, SS	For ECL I/O.
1 1 1 0 0xE	–	Combo 2	LX, GS, SS	For RS422 I/O.
1 1 1 1 0xF	–	Combo	LX, GS, SS	For ECL I/O.

* LX = PCIe8 LX / FX / SX; GS = PCI GS; SS = PCI SS; AMC = AMC FX5

APPENDIX B: Mezzanine Board FPGA Configuration Files

Overview

This appendix documents the registers for the following mezzanine board **3P** FPGA configuration files, as found in your EDT installation package.

This FPGA configuration file...	**...is used to set up the 3P mezzanine board as shown...**			
	Port 0	Port 1	Port 2	Notes
`threep_10g_sdh_sdh.bit`	10GbE	SDH	SDH	--
`threep_10g_emac_emac.bit`	10GbE	EMAC	EMAC	[‘emac’ = ethernet media access control]
`threep_stm64_sdh_sdh.bit`	STM64 / OTU	SDH	SDH	--
`threep_sdh_sdh_sync.bit`	[n/a]	SDH	SDH	[‘sync’ indicates ports 1 and 2 are synchronized]

NOTE Each 3P FPGA configuration file contains standard and extended (double indirect) registers, both fully documented.

threep_10g_sdh_sdh.bit – Standard Registers

0x00–7F [See threep.bit]

0x80–9F Port 0

0x81 Port 0 LIU Status

		Access / Notes	8-bit read-only / THREEP_P0_LIU_STATUS
			Reports the status of the 10G LIU; see link under Related Resources on page 11.
Bit	**Access**	**Name**	**Description**
7–2	–	[no name]	Reserved; reads 0.
1	R only	TX_LOCKDET	When set, the transmit phase-locked loop of the 10G LIU is locked.
0	R only	RX_LOCKDET	When set, the receive phase-locked loop of the 10G LIU is locked.

0x83 Port 0 Transceiver

		Access / Notes	8-bit read-write: 0x83 (port 0) = THREEP_P0_XCVR_STAT 0xA3 (port 1) = THREEP_P1_XCVR_STAT 0xC3 (port 2) = THREEP_P2_XCVR_STAT Enables the SFP/+ and reads their status. Defaults are adequate for normal operation; if you need to make modifications, contact EDT.
Bit	**Access**	**Name**	**Description**
7	R only	SFPP_LOS	When set, indicates loss of signal.
6	R only	SFPP_TXFAULT	When set, indicates the SFP/+ detects a fault. (If the error recurs, replace the SFP/+.)
5	R only	SFPP_PRES	When set, indicates the SFP/+ is plugged in.
4–1	–	[no name]	Reserved.
0	RW	SFPP_TXDIS	Set to disable light transmitter, if your application is receive-only.

0x84 Port 0 Enable

Access / Notes 8-bit read-write:

0x84 (port 0) = THREEP_P0_ENABLE
0xA4 (port 1) = THREEP_P1_ENABLE
0xC4 (port 2) = THREEP_P2_ENABLE

Used to initialize the clock PLLs in the correct order; see Board Architecture on page 23.

Bit	Access	Name	Description
7	R only	THREEP_TX_LOCKED	When set, indicates the transmit clock PLL is locked.
6	R only	THREEP_RX_LOCKED	When set, indicates the receive clock PLL is locked.
5	R only	SYS_LOCKED	When set, indicates the system clock PLL is locked.
4	RW	RPLL_EN	Set to operate the FPGA receive mixed mode clock manager (MMCM) normally. Clear to reset.
3–2	–	[no name]	Reserved.
1	RW	PLL_EN	Set to operate the FPGA transmit mixed mode clock manager (MMCM) normally. Clear to reset.
0	RW	LIU_EN	Set to operate the LIU normally. Clear to reset.

0x85 Port 0 Receive Framing Control

Access / Notes 8-bit read-write / THREEP_P0_RCV_FRAMING

Used to detect ethernet packets and show link and frame sync status.

Bit	Access	Name	Description
7	R only	THREEP_10GBE_LINK_GOOD	If set, a link has been established (meaning the sync header has been found and the frame sync state circuits are not in high bit error rate mode).
6	R only	THREEP_10GBE_SH_LOCK	If set, the sync header has been found.
5	R only	THREEP_10GBE_HI_BER	If set, the frame sync state circuits are in high bit error rate mode.
4	–	[no name]	Reserved.
3–2	RW	RX_DATA_SRC	00 disables the 1 GB onboard FIFO 01 enables the 1 GB onboard FIFO 1*x* test mode
1	RW	THREEP_FRAME_EN	Set to allow data collection, once the link has been established. Clear to collect raw, unsynced, scrambled data.
0	RW	THREEP_FRAME_SRCH	Set and then clear to reset the frame sync state circuits.

0x86 Port 0 Receive Filter Control

		Access / Notes	8-bit read-write / THREEP_P0_RCV_FILTER
Bit	**Access**	**Name**	**Description**
7–4	–	[no name]	Reserved.
3	RW	THREEP_10GBE_DIS_IDLE_FILT	Set to disable idle and ordered set filtering.
2–0	–	[no name]	Reserved.

0x89 Port 0 Output Data Select

		Access / Notes	8-bit read-write / THREEP_P0_OUTPUT_DATA_SEL Used for testing, to select different data sources.
Bit	**Access**	**Name**	**Description**
7	RW	THREEP_RX_PRBS	Set to receive locally generated PRBS15 data.
6	RW	THREEP_10GBE_TX_DBG_PKT	Set to transmit locally generated ethernet packets with 8-bit counter data (0x00 to 0x95) for debug purposes.
5	RW	[no name]	Set to use DDR2 FIFO to transmit; clear to use DDR2 FIFO to receive.
4	–	[no name]	Reserved.
3	RW	THREEP_PRBS_EN	Set to transmit PRBS data.
2–1	RW	THREEP_10GBE_TXDBG	Set to select transmit data source for debug purposes: "00" or "11" for normal operation with DMA through 10GBase-R PCS as data source. THREEP_10GBE_TXDBG_PCS: "01" for debug data source through 10G Base-R PCS. THREEP_10GBE_TXDBG_NOPCS: "10" for debug data source bypassing 10G Base-R PCS.
0	–	[no name]	Reserved.

0x8B Port 0 Frame Statistics Count Control

		Access / Notes	8-bit read-write: 0x8B (port 0) = THREEP_P0_CNT_CTRL 0xAB (port 1) = THREEP_P1_CNT_CTRL 0xCB (port 2) = THREEP_P2_CNT_CTRL
Bit	**Access**	**Name**	**Description**
7	RW	EN_COUNTERS	Set to enable framing error counters; clear to reset the counters
6–1	–	[no name]	Reserved.
0	RW	COUNT_HOLD	Set to hold framing error counters so that they can be read without updating; clear to update counters continuously.

0x8C Port 0 Link Fault Status

		Access / Notes	8-bit read-only / THREEP_P0_10GBE_LF_STATUS
			See registers 0x800008–09 Port 0 Local Link Fault Count and 0x80000A–0B Port 0 Remote Link Fault Count for the number of respective faults received.
Bit	**Access**	**Name**	**Description**
7–6	–	[no name]	Reserved.
5	R only	THREEP_10GBE_RT_TXLF	Real time PCS transmit local link fault.
4	R only	THREEP_10GBE_RT_RXLF	Real time PCS receive local link fault.
3–2	–	[no name]	Reserved.
1–0	R only	THREEP_10GBE_LF_MASK	Reconciliation Sublayer link fault signaling status as determined from received sequence ordered sets. "00" = OK (no fault) THREEP_10GBE_LF: "01" = local fault THREEP_10GBE_RF: "10" = remote fault THREEP_10GBE_RSVDF: "11" = reserved fault

0x8D Port 0 Loopback

		Access / Notes	8-bit read-write / THREEP_P0_10GBE_LPBK_CTRL
			Enables loopback internal to the mezzanine FPGA.
Bit	**Access**	**Name**	**Description**
7–1	–	[no name]	Reserved.
0	RW	THREEP_10GBE_LPBK_EN	Set to enable internal parallel loopback.

0x8E Port 0 PCS Control

		Access / Notes	8-bit read-write / THREEP_P0_10GBE_PCS_CTRL
Bit	**Access**	**Name**	**Description**
7–6	–	[no name]	Reserved.
5	RW	THREEP_10GBE_DIS_SCRAM	Set to bypass the transmit PCS scrambler.
4	RW	THREEP_10GBE_DIS_ENC	Set to bypass the transmit PCS encoder.
3–2	–	[no name]	Reserved.
1	RW	THREEP_10GBE_DIS_DESCRAM	Set to bypass the receive PCS descrambler.
0	RW	THREEP_10GBE_DIS_DEC	Set to bypass the receive PCS decoder.

0xA0–BF Port 1

0xA0 Port 1 Configuration 0

		Access / Notes	8-bit read-write (sets options in the SDH LIU): 0xA0 (port 1) = THREEP_P1_CONFIG0 0xC0 (port 2) = THREEP_P2_CONFIG0
Bit	**Access**	**Name**	**Description**
7	RW	PRBS_EN	When set, the LIU transmits a full-band PRBS7 code. The LIU receiver checks the code and sets a bit in 0xA2 Port 1 Status.
6	RW	LOCAL_LOOP	Sets local loopback. The port receiver is connected directly to the corresponding port transmitter.
5	RW	REMOTE_LOOP	Sets remote loopback. Data received through the fiberoptic connector is immediately transmitted out the corresponding transmit connector. The received data is also forwarded for DMA, if DMA is enabled.
4	RW	AUTO_DETECT	When this bit is set and bits 3-2 (RX_SEL) are 00, the LIU automatically detects the incoming bit rate and reports the results in 0xA2 Port 1 Status. Texas Instruments does not recommend using automatic detection.
3–2	RW	RX_SEL	Set the expected receive bit rate as follows: 00 = OC48/STM16 01 = Gigabit ethernet 10 = OC12/STM4 11 = OC3/STM1
1	RW	LOCK_REF	When set, the LIU receive clock is locked to the transmit clock internal to the LIU. For normal operation, keep this bit clear.
0	–	[no name]	Reserved.

0xA1 Port 1 Configuration 1

		Access / Notes	8-bit read-write: 0xA1 (port 1) = THREEP_P1_CONFIG1 0xC1 (port 2) = THREEP_P2_CONFIG1 Sets options in the SDH LIU; see link under Related Resources on page 11.
Bit	**Access**	**Name**	**Description**
7–5	–	[no name]	Reserved.
4	RW	LOOPTIME	Set this bit to obtain transmit timing from the receive timing. Normal 3P operation is 0 (internal timing).
3–2	RW	PRE2511	The de-emphasis level of the SDH LIU electrical interface can be programmed. For 3P operation, always set to 00.
1–0	RW	CONFG2511	The SDH LIU can be configured as follows: 00 = Full duplex transceiver, required for normal operation 01 = Transmit only 10 = Receive only 11 = Repeater mode For 3P operation, always set to 00 — full duplex transceiver.

0xA2 Port 1 Status

		Access / Notes	8-bit read-only: 0xA2 (port 1) = THREEP_P1_STATUS 0xC2 (port 2) = THREEP_P2_STATUS Sets options in the SDH LIU; see link under Related Resources on page 11.
Bit	**Access**	**Name**	**Description**
7	R only	SIG_DET	Set when the SFP transceiver module has detected an incoming signal.
6	–	[no name]	Reserved; reads 0.
5	R only	LOL	Set when the receive phase-locked loop cannot lock to the incoming data.
4	R only	LOS	Set when the SDH LIU detects loss of signal. This bit is not reset until a SONET or SDH frame is detected.
3–2	R only	RATE_DET	Bits set to the RX rate detected. Set for bit rates as follows: 00 = OC48/STM16 01 = Gigabit ethernet 10 = OC12/STM4 11 = OC3/STM1
1	R only	PRBSPASS	The receiver is receiving a valid full-band PRBS7 code as transmitted by the SDH LIU , when PRBS mode is enabled; see bit 7 (PRBS_EN) of 0xA0 Port 1 Configuration 0. The PRBS mode must be enabled, although the code can come from any source. **NOTE:** Certain bit error testers use inverted PRBS7 code.
0	R only	SPILL2511	SDH LIU transmit FIFO overflow. This can occur in loop-timing mode only if the internal transmit data clock is not the same as the received bit rate.

0xA3–A4 Port 1 [See 0x83–84]

0xA5 Port 1 Receive Framing Control

		Access / Notes	8-bit read-write: 0xA5 (port 1) = THREEP_P1_RCV_FRAMING 0xC5 (port 2) = THREEP_P2_RCV_FRAMING
Bit	**Access**	**Name**	**Description**
7	–	[no name]	Reserved.
6	RW	EN_PAR_CNT	Set to enable count of parity errors; clear to reset the counter.
5	RW	SUSPEND_AQ	Set to halt data acquisition if FIFO overflow occurs.
4	RW	DISABLE_SCRAM	Set to disable descrambling on received framed data. You must set bit 0 (FRAME_EN) and be in frame before this bit has any effect.
	RW	DISABLE_8B10B	For ethernet bit files only: Set to disable the 8b/10b decoder (see Framing on page 20).
3–2	RW	RX_DATA_SRC	00 disables the 512 MB onboard FIFO 01 enables the 512 MB onboard FIFO 1*x* test mode
1	RW	FRAME_EN	Set to allow data acquisition only when the framer is locked to the incoming signal. Collected data is also descrambled.
	RW	MAC_FILTER	Clear to acquire raw data without framing or descrambling. For ethernet bit files only: Set to align data. See also Framing on page 20.
0	RW	RESET_FRM	Set, then clear to cause the framing circuits to drop and then relock onto the framing pattern.

0xA6 Port 1 Receive Filter Control

		Access / Notes	8-bit read-write: 0x86 (port 1) = THREEP_P1_RCV_FILTER 0xC6 (port 2) = THREEP_P2_RCV_FILTER
Bit	**Access**	**Name**	**Description**
7–4	–	[no name]	Reserved.
3	RW	FORCE_ALL_DATA	For ethernet bit files only: Set to force all idles and other command symbols. See also Framing on page 20.
2–1	–	[no name]	Reserved.
0	RW	OVERHEAD_ONLY	Set to acquire SONET / SDH frame overhead only; the payload is discarded.

0xA7 Port 1 Receive Status

		Access / Notes	8-bit read-only: 0xA7 (port 1) = THREEP_P1_RCV_STATUS 0xC7 (port 2) = THREEP_P2_RCV_STATUS
Bit	**Access**	**Name**	**Description**
7–1	–	[no name]	Reserved; always reads 0.
0	R only	FRAMED	Set when incoming data is framed.

0xA8 Port 1 Receive Frame Status

		Access / Notes	8-bit read-only: 0xA8 (port 1) = THREEP_P1_RCV_FRAME_STATUS 0xC8 (port 2) = THREEP_P2_RCV_FRAME_STATUS
Bit	**Access**	**Name**	**Description**
7	R only	LOCKED	Set when frame is locked – same as bit 0 (FRAMED) in 0xA7 Port 1 Receive Status.
6	R only	FOUND	Set when frame pattern is found.
5–4	R only	DROP_CNT	The number of pattern mismatches in framer state machine.
3–2	R only	MATCH_CNT	The number of pattern matches in framer state machine.
1	R only	BYTE_SYNC	Set when the byte synchronization framing pattern is found.
0	R only	BIT_SYNC	Set when the bit synchronization framing pattern is found.

0xA9 Port 1 Transmit Framing Configuration

		Access / Notes	8-bit read-write / [no name]: 0xA9 (port 1) = THREEP_P1_XMT_FRAMING 0xC9 (port 2) = THREEP_P2_XMT_FRAMING Bits 7 and 6 work in conjunction with 0xA0 Port 1 Configuration 0, bits 3 and 2, to set up the framer.
Bit	**Access**	**Name**	**Description**
7–6	RW	[no name]	11 = OTU1 (when 0xA0 Port 1 Configuration 0 bits 3 and 2 = 00). 01 = STM*x* (when 0xA0 Port 1 Configuration 0 bits 3 and 2 have set *x* to be 1/4/16)
5	RW	[no name]	Set to initiate the transmit of the sync signal trigger.
4	–	[no name]	Reserved.
3	RW	EN_SCRAMBLE	Set to enable scrambling of output data if an OC / STM frame is detected.
2	RW	TX_FRAME_EN	Set to enable local framing with BIP error feedback. Data from the PCI bus is payload only and aligned with the AU pointer 0.
1	RW	TEST_DATA	Set to send test data; clear for normal operation.
0	RW	RESET_PTR	Toggle high, then low, to send the AU pointer reset command.

0xAA Port 1 Transmit Status

		Access / Notes	8-bit read-only: 0xAA (port 1) = THREEP_P1_TX_STATUS 0xCA (port 2) = THREEP_P2_TX_STATUS
Bit	**Access**	**Name**	**Description**
7–1	–	[no name]	Reserved (may not always read 0).
0	R only	TX_FRAMED	Set when a frame is detected in transmitted data. If scrambling is enabled in bit 3 of 0xA9 Port 1 Transmit Framing Configuration, then the data is being scrambled.

0xAB Port 1 [See 0x8B]

0xAC Port 1 B1 Error Mask

		Access / Notes	8-bit read-only: 0xAB (port 1) = THREEP_P1_B1_ERROR_MASK 0xCB (port 2) = THREEP_P2_B2_ERROR_MASK
Bit	**Access**	**Name**	**Description**
7–0	R only	[no name]	The value of the error mask for the last B1 error. A B1 error mask is one byte resulting from a logical operation on the previous frame. Errors occurring regularly in the same bit of the byte can indicate a problem in the sender's or receiver's equipment. If errors are occurring on the fiber, the B1bits in error are more likely to be randomly located in the byte.

0xAE Port 1 Receive Synchronization Control

		Access / Notes	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7	RW	[no name]	Set to arm the receive and transmit sync triggers.
6	–	[no name]	Reserved.
5	RW	[no name]	Set to use DDR2 FIFO to transmit; clear to use DDR2 FIFO to receive.
4–3	–	[no name]	Reserved.
2	RW	[no name]	Set to disable the frame align requirement for on the receive sync trigger.
1–0	RW	[no name]	Set to select trigger source. 00 = trigger from port 1.

0xAF Port 1 Transmit Synchronization Control [Reserved]

0xC0–DF Port 2 [See 0xA0–BF]

0xE0–FF Not Port-Specific

0xE0 Mezzanine FPGA Configuration File Version String

Access / Notes 8-bit read-write / [no name]

Use this register to read the FPGA configuration file version string from ROM. Write the ROM address to the register and read the ASCII data from the same register. The version string is a maximum of 64 bytes long, so only the first six bits of the address are significant.

Bit	Access	Name	Description
7–0	RW	ID_ADD_DATA	Write an address to read contents of flash memory. Result is... *bitfileName version.revision mm/dd/yyyy*

The date given is the date the FPGA configuration file was created. Replace placeholders in italics with actual values — for example, `threep_10g_sdh_sdh 1.0 08/25/2010.`

0xE1 Mezzanine FPGA Configuration File Organization

Access / Notes 8-bit read-only / [no name]

Bit	Access	Name	Description
7–0	R only	[no name]	A byte specifying the organization that created the FPGA configuration file currently loaded in the FPGA on the mezzanine board. An FPGA configuration file produced by EDT returns the value 0xFF.

0xE2–E3 Mezzanine FPGA Configuration File Design ID

Access / Notes 16-bit read-only / [no name]

This sixteen-bit number, assigned by the organization that created the FPGA configuration file as a file design ID, is loaded on the mezzanine board FPGA.

Bit	Access	Name	Description
15–0	R only	[no name]	For `threep_10g_sdh_sdh.bit,` the design ID is 0x1300.

For `threep_10g_1g_1g.bit,` the design ID is 0x1301.

For `threep_10g_emac_emac.bit,` the design ID is 0x1302.

For `threep_stm64_sdh_sdh.bit,` the design ID is 0x1303.

0xE4–E6 DDR2 Bank Status and Control

Access / Notes 8-bit read-write:

0xE4 = THREEP_BANK0A_CTRL
0xE5 = THREEP_BANK0B_CTRL
0xE6 = THREEP_BANK1_CTRL

If Bank 0A and Bank 0B are combined (as they are in the default FPGA configuration files – i.e., those with prefixes `threep_10g` and `threep_stm64`), then only Bank 0A is valid.

Bit	Access	Name	Description
7	–	[no name]	Reserved.
6	R only	PHY_INITDONE	DDR2 interface is trained.
5	R only	PLL_LOCK	Bank DDR2 interface clocks are ready.
4	R only	IDLY_RDY	IOdelay controller is ready.
3–1	–	[no name]	Reserved.
0	RW	PHY_RST	Set to reset DDR2 interface; clear to use DDR2.

0xE7 Serial Master Interface Status

Access / Notes 8-bit read-write / THREEP_SER_MASTER_DEV_ADDR

Bit	Access	Name	Description
7	R only	SER_DEV_BSY	Read only. When set, the serial master is busy.
6	R only	SER_DEV_ACK_ FAIL	Read only. When set, the serial slave failed to respond to the last command.
5–0	RW	SER_DEV_ADDR	Device 0 = SI5326: Ch0 transmit reference clock jitter attenuator Device 1 = SI570: Ch0 reference clock (transmit and receive) Device 2 = SI570: Ch1 reference clock Device 3 = SI570: Ch2 reference clock Device 4 = SFP+ EEPROM: Ch0 Device 5 = SFP+ diagnostic: Ch0 Device 6 = SFP+ EEPROM: Ch1 Device 7 = SFP+ diagnostic: Ch1 Device 8 = SFP+ EEPROM: Ch2 Device 9 = SFP+ diagnostic: Ch2 Device 10 = AMCC S19250: Ch0 LIU Device 11 = SFP ethernet PHY (electrical ethernet SFP only): Ch0 Device 12 = SFP ethernet PHY (electrical ethernet SFP only): Ch1 Device 13 = SFP ethernet PHY (electrical ethernet SFP only): Ch2

0xE8 Serial Master Interface Read

Access / Notes 8-bit read-write / THREEP_SER_MASTER_RD

Bit	Access	Name	Description
7–0	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the data returned from address.

0xE9 Serial Master Interface Register Address

		Access / Notes	8-bit read-write / THREEP_SER_MASTER_REG_ADDR
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the previously accessed serial slave register address.

0xEA Serial Master Interface Write

		Access / Notes	8-bit read-write / THREEP_SER_MASTER_WR
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Write data to the register address in register 0xE9.

0xEB–ED Time Distribution

		Access / Notes	Three 8-bit registers (for Time Distribution user's guide, see Related Resources on page 11): 0xEB on the 3P = 0x60 on the Time Distribution board. 0xEC on the 3P = 0x61 on the Time Distribution board. 0xED on the 3P = 0x62 on the Time Distribution board.

0xEE PRBS Mode

		Access / Notes	8-bit read-write / THREEP_PRBS_MODE
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Sets mode for all internal mezzanine PRBS generators and checkers.

0xF4 Frequency Counter Control

		Access / Notes	8-bit read-write / THREEP_FREQ_CNT_EN
Bit	**Access**	**Name**	**Description**
7–4	RW	[no name]	Selects the frequency counter for readback from 0xF5–F7 Frequency Counter Value. 0 = Port 0 receive clock 1 = Port 1 receive clock 2 = Port 2 receive clock 3 = Port 0 transmit clock 4 = Port 1 transmit clock 5 = Port 2 transmit clock
3–0	RW	[no name]	Set to enable port frequency counters.

0xF5–F7 Frequency Counter Value

		Access / Notes	24-bit read-only / THREEP_FREQ_CNT
Bit	**Access**	**Name**	**Description**
23–0	R	[no name]	Reads the frequency counter value, as selected in bits 7–4 of 0xF4 Frequency Counter Control.

threep_10g_sdh_sdh.bit – Extended Registers

0x800000–FF Port 0

0x800005 Port 0 Bit Error Rate Count

		Access / Notes	8-bit read-only / THREEP_P0_10GBE_BER_CNT
			Controlled by register 0x8B Port 0 Frame Statistics Count Control.
Bit	**Access**	**Name**	**Description**
7–6	–	[no name]	Reserved.
5–0	R only	[no name]	Count of invalid sync headers within current 125-microsecond period (up to 16). See IEEE Std 802.3 Clause 49.2.13.2 for details.

0x800006 Port 0 64B / 66B Decode Error Count

		Access / Notes	8-bit read-only / THREEP_P0_10GBE_DECODE_ERR_CNT
			Controlled by register 0x8B Port 0 Frame Statistics Count Control.
Bit	**Access**	**Name**	**Description**
7–0	R only	[no name]	Count of 64B / 66B decoder decode errors.

0x800008–09 Port 0 Local Link Fault Count

		Access / Notes	16-bit read-only / THREEP_P0_10GBE_LLF_CNT
			Controlled by register 0x8B Port 0 Frame Statistics Count Control.
Bit	**Access**	**Name**	**Description**
15–0	R only	[no name]	Count of received sequence ordered sets signaling a local fault.

0x80000A–0B Port 0 Remote Link Fault Count

		Access / Notes	16-bit read-only / THREEP_P0_10GBE_RLF_CNT
			Controlled by register 0x8B Port 0 Frame Statistics Count Control.
Bit	**Access**	**Name**	**Description**
15–0	R only	[no name]	Count of received sequence ordered sets signaling a remote fault.

0x800100–FF Port 1

0x800100 Port 1 Transmit National Byte

Access / Notes 8-bit read-write:

0x800100 (port 1) = THREEP_P1_XMT_NATIONAL
0x800200 (port 2) = THREEP_P2_XMT_NATIONAL

Bit	Access	Name	Description
7–0	RW	NAT_BYTE	Define byte to be sent in the National Byte field of the frame.

0x800101–04 Port 1 Transmit Test Data

Access / Notes 32-bit read-write (each access code addresses all 32 bits):

0x800101–04 (port 1) = THREEP_P1_XMT_TEST_DATA
0x800201–04 (port 2) = THREEP_P2_XMT_TEST_DATA

Bit	Access	Name	Description
31–0	RW	TEST_DATA	Bytes of a 32-bit transmit data test pattern.

0x800105–07 Port 1 B1 Error Count

Access / Notes 24-bit read-only:

0x800105–07 (port 1) = THREEP_P1_B1_ERROR_CNT
0x800205–07 (port 2) = THREEP_P2_B1_ERROR_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
23–0	R only	[no name]	The number of B1 bits found to be in error since the counter was last reset.

0x800108–0B Port 1 B2 Error Count

Access / Notes 32-bit read-only:

0x800108–0B (port 1) = THREEP_P1_B2_ERROR_CNT
0x800208–0B (port 2) = THREEP_P2_B2_ERROR_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
31–0	R only	[no name]	The number of B2 bits found to be in error since the counter was last reset.

0x80010C–0E Port 1 M1 Error Count

Access / Notes 24-bit read-only:

0x80010C–0E (port 1) = THREEP_P1_M1_ERROR_CNT
0x80020C–0E (port 2) = THREEP_P2_M1_ERROR_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
23–0	R only	[no name]	The number of M1 bits found to be in error since the counter was last reset. The M1 byte is sent from the remote receiver of the signal, if that remote receiver has detected a B1 error. In that case, the B1 error mask is copied and sent back as the M1 byte.

0x80010F–10 Port 1 Loss of Frame Count

Access / Notes 16-bit read-only:

0x80010F–10 (port 1) = THREEP_P1_LOF_CNT
0x80020F–10 (port 2) = THREEP_P2_LOF_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
15–0	R only	[no name]	The number of times framing was lost since the counter was last reset. This equals the number of times that the LOCKED bit or the FRAMED bit has gone clear (bit 7 in 0xA8 Port 1 Receive Frame Status or bit 0 in 0xA7 Port 1 Receive Status). Framing is lost when four consecutive bad framing patterns are detected.

0x800111–12 Port 1 Frame Pattern Error Count

Access / Notes 16-bit read-only:

0x800111–12 (port 1) = THREEP_P1_FRM_PAT_CNT
0x800211–12 (port 2) = THREEP_P2_FRM_PAT_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
15–0	R only	[no name]	The number of times that the framing pattern was not correct, after data has been in frame. Because framing is not lost until the framing pattern has been incorrect four consecutive times, an incorrect framing pattern does not necessarily mean that framing was lost.

0x800113–14 Port 1 False Frame Count

Access / Notes 16-bit read-only:

0x800113–14 (port 1) = THREEP_P1_FALSE_FRM_CNT
0x800213–14 (port 2) = THREEP_P2_FALSE_FRM_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
15–0	R only	[no name]	When searching for frame, the number of times that a possible frame pattern was detected but the signal was not framed. This can be useful for distinguishing whether the signal sometimes appears to be framed, or whether it always appears to be unframed, and therefore possibly gibberish.

0x800115 Port 1 Demux Bitmap

Access / Notes 8-bit read-write:

0x800115 (port 1) = THREEP_P1_DEMUX_BITMAP
0x800215 (port 2) = THREEP_P2_DEMUX_BITMAP

This register addresses a 48-bit mask register that is accessed via twelve 4-bit writes. The top four bits address the desired 4 bits of the mask register, while the bottom four bits are the value written.

Bit 3 of address 0 disables the first byte of each 48-byte OC48/STM16 multiplexed group, and bit 0 of address B disables the last byte of each multiplexed group. To enable all bytes of the group, all bits are 0 (the default).

Bit	Access	Name	Description
7–4	RW	MASK_ADDR	Bit register address 0x00–0B.
3–0	RW	DEMUX_MASK	Bitmask. A value of 1 masks the corresponding byte of each 48-byte multiplexed group.

STM1
enabling AU-3(1)

The mask is written 4 bits at a time; only bits 3–1 of the mask are used.

Example: To select AU-3(1), the first AU-3, use the `pdb` command...

: iw 800115 07

STM4
enabling STM1(1,0)

The mask is written 4 bits at a time; only the first 12 bits of the mask are used.

Example: To select AU-4(1,0), the first STM1, use the `pdb` commands...

: iw 800115 07
: iw 800115 17
: iw 800115 27

STM16
enabling STM1(1,1,0)

The mask is written 4 bits at a time; only the first 48 bits of the mask are used.

Example: To select AU-4(1,1,0), the first STM1, use the `pdb` commands...

: iw 800115 07
: iw 800115 1F
: iw 800115 2F
: iw 800115 3F
: iw 800115 47
: iw 800115 5F
: iw 800115 6F
: iw 800115 7F
: iw 800115 87
: iw 800115 9F
: iw 800115 AF
: iw 800115 BF

0x800116 Port 1 Demux Bitmap Readback

Access / Notes 8-bit read-write:

0x800116 (port 1) = THREEP_P1_DEMUX_BITMAP_READ
0x800216 (port 2) = THREEP_P2_DEMUX_BITMAP_READ

Reads back the demultiplexing bitmask. Write this register with the address of the 4-bit mask you wish to read. Read the stored bit pattern in the bottom four bits.

Bit	Access	Name	Description
7–4	RW	MASK_ADDR	Bit register address 0x00 – 0x0B.
3–0	RW	DEMUX_MASK	The bitmask. A value of 1 masks the corresponding byte of each 48-byte multiplexed group.

0x800200–FF Port 2 [See 0x800100–FF]

threep_10g_emac_emac.bit – Standard Registers

0x00–7F [See threep.bit]

0x80–9F Port 0

0x80–9F Port 0

0x81 Port 0 LIU Status

		Access / Notes	8-bit read-only / THREEP_P0_LIU_STATUS
			Reports the status of the 10G LIU; see link under Related Resources on page 11.
Bit	**Access**	**Name**	**Description**
7–2	–	[no name]	Reserved; reads 0.
1	R only	TX_LOCKDET	When set, the transmit phase-locked loop of the 10G LIU is locked.
0	R only	RX_LOCKDET	When set, the receive phase-locked loop of the 10G LIU is locked.

0x83 Port 0 Transceiver

		Access / Notes	8-bit read-write: 0x83 (port 0) = THREEP_P0_XCVR_STAT 0xA3 (port 1) = THREEP_P1_XCVR_STAT 0xC3 (port 2) = THREEP_P2_XCVR_STAT Enables the SFP/+ and reads their status. Defaults are adequate for normal operation; if you need to make modifications, contact EDT.
Bit	**Access**	**Name**	**Description**
7	R only	SFPP_LOS	When set, indicates loss of signal.
6	R only	SFPP_TXFAULT	When set, indicates the SFP/+ detects a fault. (If the error recurs, replace the SFP/+.)
5	R only	SFPP_PRES	When set, indicates the SFP/+ is plugged in.
4–1	–	[no name]	Reserved.
0	RW	SFPP_TXDIS	Set to disable light transmitter, if your application is receive-only.

0x84 Port 0 Enable

Access / Notes 8-bit read-write:

0x84 (port 0) = THREEP_P0_ENABLE
0xA4 (port 1) = THREEP_P1_ENABLE
0xC4 (port 2) = THREEP_P2_ENABLE

Used to initialize the clock PLLs in the correct order; see Board Architecture on page 23.

Bit	Access	Name	Description
7	R only	THREEP_TX_LOCKED	When set, indicates the transmit clock PLL is locked.
6	R only	THREEP_RX_LOCKED	When set, indicates the receive clock PLL is locked.
5	R only	SYS_LOCKED	When set, indicates the system clock PLL is locked.
4	RW	RPLL_EN	Set to operate the FPGA receive mixed mode clock manager (MMCM) normally. Clear to reset.
3–2	–	[no name]	Reserved.
1	RW	PLL_EN	Set to operate the FPGA transmit mixed mode clock manager (MMCM) normally. Clear to reset.
0	RW	LIU_EN	Set to operate the LIU normally. Clear to reset.

0x85 Port 0 Receive Framing Control

Access / Notes 8-bit read-write / THREEP_P0_RCV_FRAMING

Used to detect ethernet packets and show link and frame sync status.

Bit	Access	Name	Description
7	R only	THREEP_10GBE_LINK_GOOD	If set, a link has been established (meaning the sync header has been found and the frame sync state circuits are not in high bit error rate mode).
6	R only	THREEP_10GBE_SH_LOCK	If set, the sync header has been found.
5	R only	THREEP_10GBE_HI_BER	If set, the frame sync state circuits are in high bit error rate mode.
4	–	[no name]	Reserved.
3–2	RW	RX_DATA_SRC	00 disables the 1 GB onboard FIFO 01 enables the 1 GB onboard FIFO 1*x* test mode
1	RW	THREEP_FRAME_EN	Set to allow data collection, once the link has been established. Clear to collect raw, unsynced, scrambled data.
0	RW	THREEP_FRAME_SRCH	Set and then clear to reset the frame sync state circuits.

0x86 Port 0 Receive Filter Control

		Access / Notes	8-bit read-write / THREEP_P0_RCV_FILTER
Bit	**Access**	**Name**	**Description**
7–4	–	[no name]	Reserved.
3	RW	THREEP_10GBE_DIS_IDLE_FILT	Set to disable idle and ordered set filtering.
2–0	–	[no name]	Reserved.

0x89 Port 0 Output Data Select

		Access / Notes	8-bit read-write / THREEP_P0_OUTPUT_DATA_SEL Used for testing, to select different data sources.
Bit	**Access**	**Name**	**Description**
7	RW	THREEP_RX_PRBS	Set to receive locally generated PRBS15 data.
6	RW	THREEP_10GBE_TX_DBG_PKT	Set to transmit locally generated ethernet packets with 8-bit counter data (0x00 to 0x95) for debug purposes.
5	RW	[no name]	Set to use DDR2 FIFO to transmit; clear to use DDR2 FIFO to receive.
4	–	[no name]	Reserved.
3	RW	THREEP_PRBS_EN	Set to transmit PRBS data.
2–1	RW	THREEP_10GBE_TXDBG	Set to select transmit data source for debug purposes: "00" or "11" for normal operation with DMA through 10GBase-R PCS as data source. THREEP_10GBE_TXDBG_PCS: "01" for debug data source through 10G Base-R PCS. THREEP_10GBE_TXDBG_NOPCS: "10" for debug data source bypassing 10G Base-R PCS.
0	–	[no name]	Reserved.

0x8B Port 0 Frame Statistics Count Control

		Access / Notes	8-bit read-write: 0x8B (port 0) = THREEP_P0_CNT_CTRL 0xAB (port 1) = THREEP_P1_CNT_CTRL 0xCB (port 2) = THREEP_P2_CNT_CTRL
Bit	**Access**	**Name**	**Description**
7	RW	EN_COUNTERS	Set to enable framing error counters; clear to reset the counters
6–1	–	[no name]	Reserved.
0	RW	COUNT_HOLD	Set to hold framing error counters so that they can be read without updating; clear to update counters continuously.

0x8C Port 0 Link Fault Status

		Access / Notes	8-bit read-only / THREEP_P0_10GBE_LF_STATUS
			See registers 0x800008–09 Port 0 Local Link Fault Count and 0x80000A–0B Port 0 Remote Link Fault Count for the number of respective faults received.
Bit	**Access**	**Name**	**Description**
7–6	–	[no name]	Reserved.
5	R only	THREEP_10GBE_RT_TXLF	Real time PCS transmit local link fault.
4	R only	THREEP_10GBE_RT_RXLF	Real time PCS receive local link fault.
3–2	–	[no name]	Reserved.
1–0	R only	THREEP_10GBE_LF_MASK	Reconciliation Sublayer link fault signaling status as determined from received sequence ordered sets. "00" = OK (no fault) THREEP_10GBE_LF: "01" = local fault THREEP_10GBE_RF: "10" = remote fault THREEP_10GBE_RSVDF: "11" = reserved fault

0x8D Port 0 Loopback

		Access / Notes	8-bit read-write / THREEP_P0_10GBE_LPBK_CTRL
			Enables loopback internal to the mezzanine FPGA.
Bit	**Access**	**Name**	**Description**
7–1	–	[no name]	Reserved.
0	RW	THREEP_10GBE_LPBK_EN	Set to enable internal parallel loopback.

0x8E Port 0 PCS Control

		Access / Notes	8-bit read-write / THREEP_P0_10GBE_PCS_CTRL
Bit	**Access**	**Name**	**Description**
7–6	–	[no name]	Reserved.
5	RW	THREEP_10GBE_DIS_SCRAM	Set to bypass the transmit PCS scrambler.
4	RW	THREEP_10GBE_DIS_ENC	Set to bypass the transmit PCS encoder.
3–2	–	[no name]	Reserved.
1	RW	THREEP_10GBE_DIS_DESCRAM	Set to bypass the receive PCS descrambler.
0	RW	THREEP_10GBE_DIS_DEC	Set to bypass the receive PCS decoder.

0xA0–BF Port 1

0xA3–A4 Port 1 [See 0x83–84 Port 0]

0xA5 Port 1 Receive Framing Control

		Access / Notes	8-bit read-write / THREEP_P1_RCV_FRAMING
			0xA5 (port 1) = THREEP_P1_RCV_FRAMING 0xC5 (port 2) = THREEP_P2_RCV_FRAMING
Bit	**Access**	**Name**	**Description**
7–4	–	[no name]	Reserved.
3–2	RW	RX_DATA_SRC	00 disables the 1 GB onboard FIFO
			01 enables the 1 GB onboard FIFO
			1*x* test mode
1–0	–	[no name]	Reserved.

0xAB Port 1 Transmit Pre-cursor Pre-emphasis and Driver Swing Control

Access / Notes 8-bit read-write / [no name]

0xAB (port 1)
0xCB (port 2)

See the Xilinx user guide for the Virtex 6 FPGA GTX transceivers (document #UG366).

Bit	Access	Name	Description
7–4	RW	[no name]	Transmitter pre-cursor TX pre-emphasis control.
3–0	RW	[no name]	Driver swing control.

0xAC Port 1 Transmit Post-cursor Pre-emphasis

Access / Notes 8-bit read-write / [no name]

0xAC (port 1)
0xCC (port 2)

See the Xilinx user guide for the Virtex 6 FPGA GTX transceivers (document #UG366).

Bit	Access	Name	Description
7–5	–	[no name]	Reserved.
4–0	RW	[no name]	Transmitter post-cursor pre-emphasis control.

0xAD–B0 Port 1 [Reserved]

0xB1–B2 Port 1 EMAC and MDIO Register Address

Access / Notes 16-bit read-write / THREEP_EMAC_HOSTREG_ADDR

0xB1–B2 (port 1) = THREEP_EMAC_HOSTREG_ADDR + 1 (port number) * 0x20
0xD1–D2 (port 2) = THREEP_EMAC_HOSTREG_ADDR + 2 (port number) * 0x20

For details about the EMAC register space, see the Xilinx user guide for the Virtex 6 FPGA embedded tri-mode ethernet MAC (document #UG368).

Writing to this register sets the EMAC or MDIO register address and initiates a register read.

Bit	Access	Name	Description
15–13	–	[no name]	Reserved.
12	RW	[no name]	Set to address MDIO registers; clear to address EMAC registers.
11–10	–	[no name]	Reserved.
9–0	RW	[no name]	EMAC / MDIO register address.

0xB3–B6 Port 1 EMAC and MDIO Register Data

Access / Notes 32-bit read-write / THREEP_EMAC_HOSTREG_DATA

0xB3–B6 (port 1) = THREEP_EMAC_HOSTREG_DATA + 1 (port number) * 0x20
0xD3–D6 (port 2) = THREEP_EMAC_HOSTREG_DATA + 2 (port number) * 0x20

For details about the EMAC register space, see the Xilinx user guide for the Virtex 6 FPGA embedded tri-mode ethernet MAC (document #UG368).

Writing to this register initiates a write to the EMAC or MDIO register addressed in 0xB1–B2. Reading from this register reads the last register read or write.

Bit	Access	Name	Description
31–0	RW	[no name]	EMAC / MDIO register data.

0xC0–DF Port 2

0xC3–C5 Port 2 [See 0xA3–A5]

0xCB–CC Port 2 [See 0xAB–AC]

0xD1–D6 Port 2 [See 0xB1–B6]

0xE0–FF Not Port-Specific

0xE0 Mezzanine FPGA Configuration File Version String

Access / Notes 8-bit read-write / [no name]

Use this register to read the FPGA configuration file version string from ROM. Write the ROM address to the register and read the ASCII data from the same register. The version string is a maximum of 64 bytes long, so only the first six bits of the address are significant.

Bit	Access	Name	Description
7–0	RW	ID_ADD_DATA	Write an address to read contents of flash memory. Result is... *bitfileName version.revision mm/dd/yyyy*

The date given is the date the FPGA configuration file was created. Replace placeholders in italics with actual values — for example, `threep_10g_sdh_sdh 1.0 08/25/2010.`

0xE1 Mezzanine FPGA Configuration File Organization

		Access / Notes	8-bit read-only / [no name]
Bit	**Access**	**Name**	**Description**
7–0	R only	[no name]	A byte specifying the organization that created the FPGA configuration file currently loaded in the FPGA on the mezzanine board. An FPGA configuration file produced by EDT returns the value 0xFF.

0xE2–E3 Mezzanine FPGA Configuration File Design ID

		Access / Notes	16-bit read-only / [no name]
			This sixteen-bit number, assigned by the organization that created the FPGA configuration file as a file design ID, is loaded on the mezzanine board FPGA.
Bit	**Access**	**Name**	**Description**
15–0	R only	[no name]	For `threep_10g_sdh_sdh.bit,` the design ID is 0x1300.
			For `threep_10g_1g_1g.bit,` the design ID is 0x1301.
			For `threep_10g_emac_emac.bit,` the design ID is 0x1302.
			For `threep_stm64_sdh_sdh.bit,` the design ID is 0x1303.

0xE4–E6 DDR2 Bank Status and Control

		Access / Notes	8-bit read-write:
			0xE4 = THREEP_BANK0A_CTRL 0xE5 = THREEP_BANK0B_CTRL 0xE6 = THREEP_BANK1_CTRL
			If Bank 0A and Bank 0B are combined (as they are in the default FPGA configuration files – i.e., those with prefixes `threep_10g` and `threep_stm64`), then only Bank 0A is valid.
Bit	**Access**	**Name**	**Description**
7	–	[no name]	Reserved.
6	R only	PHY_INITDONE	DDR2 interface is trained.
5	R only	PLL_LOCK	Bank DDR2 interface clocks are ready.
4	R only	IDLY_RDY	IOdelay controller is ready.
3–1	–	[no name]	Reserved.
0	RW	PHY_RST	Set to reset DDR2 interface; clear to use DDR2.

0xE7 Serial Master Interface Status

		Access / Notes	8-bit read-write / THREEP_SER_MASTER_DEV_ADDR
Bit	**Access**	**Name**	**Description**
7	R only	SER_DEV_BSY	Read only. When set, the serial master is busy.
6	R only	SER_DEV_ACK_ FAIL	Read only. When set, the serial slave failed to respond to the last command.
5–0	RW	SER_DEV_ADDR	Device 0 = SI5326: Ch0 transmit reference clock jitter attenuator Device 1 = SI570: Ch0 reference clock (transmit and receive) Device 2 = SI570: Ch1 reference clock Device 3 = SI570: Ch2 reference clock Device 4 = SFP+ EEPROM: Ch0 Device 5 = SFP+ diagnostic: Ch0 Device 6 = SFP+ EEPROM: Ch1 Device 7 = SFP+ diagnostic: Ch1 Device 8 = SFP+ EEPROM: Ch2 Device 9 = SFP+ diagnostic: Ch2 Device 10 = AMCC S19250: Ch0 LIU Device 11 = SFP ethernet PHY (electrical ethernet SFP only): Ch0 Device 12 = SFP ethernet PHY (electrical ethernet SFP only): Ch1 Device 13 = SFP ethernet PHY (electrical ethernet SFP only): Ch2

0xE8 Serial Master Interface Read

		Access / Notes	8-bit read-write / THREEP_SER_MASTER_RD
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the data returned from address.

0xE9 Serial Master Interface Register Address

		Access / Notes	8-bit read-write / THREEP_SER_MASTER_REG_ADDR
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the previously accessed serial slave register address.

0xEA Serial Master Interface Write

		Access / Notes	8-bit read-write / THREEP_SER_MASTER_WR
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Write data to the register address in register 0xE9.

0xEB–ED Time Distribution

Access / Notes Three 8-bit registers (for Time Distribution user's guide, see Related Resources on page 11):

0xEB on the 3P = 0x60 on the Time Distribution board.
0xEC on the 3P = 0x61 on the Time Distribution board.
0xED on the 3P = 0x62 on the Time Distribution board.

0xEE PRBS Mode

Access / Notes 8-bit read-write / THREEP_PRBS_MODE

Bit	Access	Name	Description
7–0	RW	[no name]	Sets mode for all internal mezzanine PRBS generators and checkers.

0xF4 Frequency Counter Control

Access / Notes 8-bit read-write / THREEP_FREQ_CNT_EN

Bit	Access	Name	Description
7–4	RW	[no name]	Selects the frequency counter for readback from 0xF5–F7 Frequency Counter Value. 0 = Port 0 receive clock 1 = Port 1 receive clock 2 = Port 2 receive clock 3 = Port 0 transmit clock 4 = Port 1 transmit clock 5 = Port 2 transmit clock
3–0	RW	[no name]	Set to enable port frequency counters.

0xF5–F7 Frequency Counter Value

Access / Notes 24-bit read-only / THREEP_FREQ_CNT

Bit	Access	Name	Description
23–0	R	[no name]	Reads the frequency counter value, as selected in bits 7–4 of 0xF4 Frequency Counter Control.

threep_10g_emac_emac.bit – Extended Registers

0x800000–FF Port 0

0x800005 Port 0 Bit Error Rate Count

		Access / Notes	8-bit read-only / THREEP_P0_10GBE_BER_CNT
			Controlled by register 0x8B Port 0 Frame Statistics Count Control.
Bit	**Access**	**Name**	**Description**
7–6	–	[no name]	Reserved.
5–0	R only	[no name]	Count of invalid sync headers within current 125-microsecond period (up to 16). See IEEE Std 802.3 Clause 49.2.13.2 for details.

0x800006 Port 0 64B / 66B Decode Error Count

		Access / Notes	8-bit read-only / THREEP_P0_10GBE_DECODE_ERR_CNT
			Controlled by register 0x8B Port 0 Frame Statistics Count Control.
Bit	**Access**	**Name**	**Description**
7–0	R only	[no name]	Count of 64B / 66B decoder decode errors.

0x800008–09 Port 0 Local Link Fault Count

		Access / Notes	16-bit read-only / THREEP_P0_10GBE_LLF_CNT
			Controlled by register 0x8B Port 0 Frame Statistics Count Control.
Bit	**Access**	**Name**	**Description**
15–0	R only	[no name]	Count of received sequence ordered sets signaling a local fault.

0x80000A–0B Port 0 Remote Link Fault Count

		Access / Notes	16-bit read-only / THREEP_P0_10GBE_RLF_CNT
			Controlled by register 0x8B Port 0 Frame Statistics Count Control.
Bit	**Access**	**Name**	**Description**
15–0	R only	[no name]	Count of received sequence ordered sets signaling a remote fault.

0x800100–FF Port 1 [Reserved]

0x800200–FF Port 2 [Reserved]

threep_stm64_sdh_sdh.bit – Standard Registers

0x00–7F [See threep.bit]

0x80–9F Port 0

0x81 Port 0 LIU Status

		Access / Notes	8-bit read-only / THREEP_P0_LIU_STATUS
			Reports the status of the 10G LIU; see link under Related Resources on page 11.
Bit	**Access**	**Name**	**Description**
7–2	–	[no name]	Reserved; reads 0.
1	R only	TX_LOCKDET	When set, the transmit phase-locked loop of the 10G LIU is locked.
0	R only	RX_LOCKDET	When set, the receive phase-locked loop of the 10G LIU is locked.

0x83 Port 0 Transceiver

		Access / Notes	8-bit read-write: 0x83 (port 0) = THREEP_P0_XCVR_STAT 0xA3 (port 1) = THREEP_P1_XCVR_STAT 0xC3 (port 2) = THREEP_P2_XCVR_STAT Enables the SFP/+ and reads their status. Defaults are adequate for normal operation; if you need to make modifications, contact EDT.
Bit	**Access**	**Name**	**Description**
7	R only	SFPP_LOS	When set, indicates loss of signal.
6	R only	SFPP_TXFAULT	When set, indicates the SFP/+ detects a fault. (If the error recurs, replace the SFP/+.)
5	R only	SFPP_PRES	When set, indicates the SFP/+ is plugged in.
4–1	–	[no name]	Reserved.
0	RW	SFPP_TXDIS	Set to disable light transmitter, if your application is receive-only.

0x84 Port 0 Enable

		Access / Notes	8-bit read-write: 0x84 (port 0) = THREEP_P0_ENABLE 0xA4 (port 1) = THREEP_P1_ENABLE 0xC4 (port 2) = THREEP_P2_ENABLE Used to initialize the clock PLLs in the correct order; see Board Architecture on page 23.
Bit	**Access**	**Name**	**Description**
7	R only	THREEP_TX_ LOCKED	When set, indicates the transmit clock PLL is locked.
6	R only	THREEP_RX_ LOCKED	When set, indicates the receive clock PLL is locked.
5	R only	SYS_LOCKED	When set, indicates the system clock PLL is locked.
4	RW	RPLL_EN	Set to operate the FPGA receive mixed mode clock manager (MMCM) normally. Clear to reset.
3–2	–	[no name]	Reserved.
1	RW	PLL_EN	Set to operate the FPGA transmit mixed mode clock manager (MMCM) normally. Clear to reset.
0	RW	LIU_EN	Set to operate the LIU normally. Clear to reset.

0x85 Port 0 Receive Framing Control

		Access / Notes	8-bit read-write / THREEP_P0_RCV_FRAMING
Bit	**Access**	**Name**	**Description**
7	R only	FRAME_LOCK	When set, the framing engine has locked onto the incoming SONET / SDH or OTU data stream.
6	R only	BYTE_SYNC	When set, the byte synchronization framing pattern has been found.
5	R only	BIT_SYNC	When set, the bit synchronization framing pattern has been found.
4	RW	DISABLE_SCRAM	Set to disable descrambling on framed data. Bit 1 must be set before the descrambler can be disabled.
3–2	RW	[no name]	00 = disables the 1GB onboard FIFO. 01 = enables the 1GB onboard FIFO. 1x = reserved.
1	RW	FRAME_EN	Set to allow the data acquisition only when the framer is locked to the incoming signal.
0	RW	SEARCH	Set, then clear, to cause the framing circuits to drop and then relock onto the framing pattern.

0x86 Port 0 Receive Filter Control

		Access / Notes	8-bit read-write / THREEP_P0_RCV_FILTER
Bit	**Access**	**Name**	**Description**
7–4	–	[no name]	Reserved.
3	RW	[no name]	Set to enable PRBS checker on payload only (for debugging purposes).
2	RW	[no name]	Set to acquire SONET / SDH frame payload only.
1	–	[no name]	Reserved.
0	RW	OVERHEAD_ONLY	Set to acquire SONET / SDH frame overhead only, when framing is enabled (the payload is discarded).

0x89 Port 0 Output Data Control

		Access / Notes	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7–6	–	[no name]	Reserved.
5	RW	[no name]	Set to use the 1GB DDR2 FIFO for transmit.
4	RW	[no name]	Set to enable SOH generation on transmit.
3–0	–	[no name]	Reserved.

0x8B Port 0 Frame Statistics Count Control

		Access / Notes	8-bit read-write: 0x8B (port 0) = THREEP_P0_CNT_CTRL 0xAB (port 1) = THREEP_P1_CNT_CTRL 0xCB (port 2) = THREEP_P2_CNT_CTRL
Bit	**Access**	**Name**	**Description**
7	RW	EN_COUNTERS	Set to enable framing error counters; clear to reset the counters
6–1	–	[no name]	Reserved.
0	RW	COUNT_HOLD	Set to hold framing error counters so that they can be read without updating; clear to update counters continuously.

0x8C Port 0 B1 Error Mask

		Access / Notes	8-bit read-only / THREEP_P0_B1_ERROR_MASK
Bit	**Access**	**Name**	**Description**
7–0	R only	[no name]	The value of the error mask for the last B1 error. A B1 error mask is one byte resulting from a logical operation on the previous frame. Errors occurring regularly in the same bit of the byte can indicate a problem in the sender's or receiver's equipment. If errors are occurring on the fiber, the B1bits in error are more likely to be randomly located in the byte.

0x8D Port 0 Frame Tagging

		Access / Notes	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7	RW	[no name]	Set to enable frame tagging.
6	RW	[no name]	Set to save tagged frames.
5–4	–	[no name]	Reserved.
3–0	RW	[no name]	Set tag ID.

0x8E Port 0 Receive Synchronization Control

		Access / Notes	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7	RW	[no name]	Set to arm the receive and transmit synchronization triggers.
6–3	–	[no name]	Reserved.
2	RW	[no name]	Set to disable the frame align requirement for the receive synchronization trigger.
1–0	RW	[no name]	Set to select the trigger source: 00 = trigger from port 1.

0x8F Port 0 Transmit Synchronization Control [Reserved]

0x90 Port 0 [Reserved]

0x91 Port 1 Framer Rate Select

		Access / Notes	8-bit read-write / THREEP_P0_FRAMER_RATE
Bit	**Access**	**Name**	**Description**
7–3	–	[no name]	Reserved.
2–0	RW	[no name]	000 = OC 192 / STM64 Other - OTU2 / 2e / 2f

0xA0–BF Port 1

0xA0 Port 1 Configuration 0

		Access / Notes	8-bit read-write (sets options in the SDH LIU): 0xA0 (port 1) = THREEP_P1_CONFIG0 0xC0 (port 2) = THREEP_P2_CONFIG0
Bit	**Access**	**Name**	**Description**
7	RW	PRBS_EN	When set, the LIU transmits a full-band PRBS7 code. The LIU receiver checks the code and sets a bit in 0xA2 Port 1 Status.
6	RW	LOCAL_LOOP	Sets local loopback. The port receiver is connected directly to the corresponding port transmitter.
5	RW	REMOTE_LOOP	Sets remote loopback. Data received through the fiberoptic connector is immediately transmitted out the corresponding transmit connector. The received data is also forwarded for DMA, if DMA is enabled.
4	RW	AUTO_DETECT	When this bit is set and bits 3-2 (RX_SEL) are 00, the LIU automatically detects the incoming bit rate and reports the results in 0xA2 Port 1 Status. Texas Instruments does not recommend using automatic detection.
3–2	RW	RX_SEL	Set the expected receive bit rate as follows: 00 = OC48/STM16 01 = Gigabit ethernet 10 = OC12/STM4 11 = OC3/STM1
1	RW	LOCK_REF	When set, the LIU receive clock is locked to the transmit clock internal to the LIU. For normal operation, keep this bit clear.
0	–	[no name]	Reserved.

0xA1 Port 1 Configuration 1

		Access / Notes	8-bit read-write: 0xA1 (port 1) = THREEP_P1_CONFIG1 0xC1 (port 2) = THREEP_P2_CONFIG1 Sets options in the SDH LIU; see link under Related Resources on page 11.
Bit	**Access**	**Name**	**Description**
7–5	–	[no name]	Reserved.
4	RW	LOOPTIME	Set this bit to obtain transmit timing from the receive timing. Normal 3P operation is 0 (internal timing).
3–2	RW	PRE2511	The de-emphasis level of the SDH LIU electrical interface can be programmed. For 3P operation, always set to 00.
1–0	RW	CONFG2511	The SDH LIU can be configured as follows: 00 = Full duplex transceiver, required for normal operation 01 = Transmit only 10 = Receive only 11 = Repeater mode For 3P operation, always set to 00 — full duplex transceiver.

0xA2 Port 1 Status

Access / Notes 8-bit read-only:

0xA2 (port 1) = THREEP_P1_STATUS
0xC2 (port 2) = THREEP_P2_STATUS

Sets options in the SDH LIU; see link under Related Resources on page 11.

Bit	Access	Name	Description
7	R only	SIG_DET	Set when the SFP transceiver module has detected an incoming signal.
6	–	[no name]	Reserved; reads 0.
5	R only	LOL	Set when the receive phase-locked loop cannot lock to the incoming data.
4	R only	LOS	Set when the SDH LIU detects loss of signal. This bit is not reset until a SONET or SDH frame is detected.
3–2	R only	RATE_DET	Bits set to the RX rate detected. Set for bit rates as follows: 00 = OC48/STM16 01 = Gigabit ethernet 10 = OC12/STM4 11 = OC3/STM1
1	R only	PRBSPASS	The receiver is receiving a valid full-band PRBS7 code as transmitted by the SDH LIU , when PRBS mode is enabled; see bit 7 (PRBS_EN) of 0xA0 Port 1 Configuration 0. The PRBS mode must be enabled, although the code can come from any source. **NOTE:** Certain bit error testers use inverted PRBS7 code.
0	R only	SPILL2511	SDH LIU transmit FIFO overflow. This can occur in loop-timing mode only if the internal transmit data clock is not the same as the received bit rate.

0xA3–A4 Port 1 [See 0x83–84]

0xA5 Port 1 Receive Framing Control

Access / Notes 8-bit read-write:

0xA5 (port 1) = THREEP_P1_RCV_FRAMING
0xC5 (port 2) = THREEP_P2_RCV_FRAMING

Bit	Access	Name	Description
7	–	[no name]	Reserved.
6	RW	EN_PAR_CNT	Set to enable count of parity errors; clear to reset the counter.
5	RW	SUSPEND_AQ	Set to halt data acquisition if FIFO overflow occurs.
4	RW	DISABLE_SCRAM	Set to disable descrambling on received framed data. You must set bit 0 (FRAME_EN) and be in frame before this bit has any effect.
3–2	RW	RX_DATA_SRC	00 disables the 512 MB onboard FIFO 01 enables the 512 MB onboard FIFO 1*x* test mode
1	RW	FRAME_EN	Set to allow data acquisition only when the framer is locked to the incoming signal. Collected data is also descrambled.
0	RW	RESET_FRM	Set, then clear to cause the framing circuits to drop and then relock onto the framing pattern.

0xA6 Port 1 Receive Filter Control

		Access / Notes	8-bit read-write: 0x86 (port 1) = THREEP_P1_RCV_FILTER 0xC6 (port 2) = THREEP_P2_RCV_FILTER
Bit	**Access**	**Name**	**Description**
7–1	–	[no name]	Reserved.
0	RW	OVERHEAD_ONLY	Set to acquire SONET / SDH frame overhead only; the payload is discarded.

0xA7 Port 1 Receive Status

		Access / Notes	8-bit read-only: 0xA7 (port 1) = THREEP_P1_RCV_STATUS 0xC7 (port 2) = THREEP_P2_RCV_STATUS
Bit	**Access**	**Name**	**Description**
7–1	–	[no name]	Reserved; always reads 0.
0	R only	FRAMED	Set when incoming data is framed.

0xA8 Port 1 Receive Frame Status

		Access / Notes	8-bit read-only: 0xA8 (port 1) = THREEP_P1_RCV_FRAME_STATUS 0xC8 (port 2) = THREEP_P2_RCV_FRAME_STATUS
Bit	**Access**	**Name**	**Description**
7	R only	LOCKED	Set when frame is locked – same as bit 0 (FRAMED) in 0xA7 Port 1 Receive Status.
6	R only	FOUND	Set when frame pattern is found.
5–4	R only	DROP_CNT	The number of pattern mismatches in framer state machine.
3–2	R only	MATCH_CNT	The number of pattern matches in framer state machine.
1	R only	BYTE_SYNC	Set when the byte synchronization framing pattern is found.
0	R only	BIT_SYNC	Set when the bit synchronization framing pattern is found.

0xA9 Port 1 Transmit Framing Configuration

Access / Notes 8-bit read-write / [no name]:

0xA9 (port 1) = THREEP_P1_XMT_FRAMING
0xC9 (port 2) = THREEP_P2_XMT_FRAMING

Bits 7 and 6 work in conjunction with 0xA0 Port 1 Configuration 0, bits 3 and 2, to set up the framer.

Bit	Access	Name	Description
7–6	RW	[no name]	11 = OTU1 (when 0xA0 Port 1 Configuration 0 bits 3 and 2 = 00). 01 = STM*x* (when 0xA0 Port 1 Configuration 0 bits 3 and 2 have set *x* to be 1/4/16)
5	RW	[no name]	Set to initiate the transmit of the sync signal trigger.
4	–	[no name]	Reserved.
3	RW	EN_SCRAMBLE	Set to enable scrambling of output data if an OC / STM frame is detected.
2	RW	TX_FRAME_EN	Set to enable local framing with BIP error feedback. Data from the PCI bus is payload only and aligned with the AU pointer 0.
1	RW	TEST_DATA	Set to send test data; clear for normal operation.
0	RW	RESET_PTR	Toggle high, then low, to send the AU pointer reset command.

0xAA Port 1 Transmit Status

Access / Notes 8-bit read-only:

0xAA (port 1) = THREEP_P1_TX_STATUS
0xCA (port 2) = THREEP_P2_TX_STATUS

Bit	Access	Name	Description
7–1	–	[no name]	Reserved (may not always read 0).
0	R only	TX_FRAMED	Set when a frame is detected in transmitted data. If scrambling is enabled in bit 3 of 0xA9 Port 1 Transmit Framing Configuration, then the data is being scrambled.

0xAB Port 1 [See 0x8B]

0xAC Port 1 B1 Error Mask

Access / Notes 8-bit read-only:

0xAB (port 1) = THREEP_P1_B1_ERROR_MASK
0xCB (port 2) = THREEP_P2_B1_ERROR_MASK

Bit	Access	Name	Description
7–0	R only	[no name]	The value of the error mask for the last B1 error. A B1 error mask is one byte resulting from a logical operation on the previous frame. Errors occurring regularly in the same bit of the byte can indicate a problem in the sender's or receiver's equipment. If errors are occurring on the fiber, the B1bits in error are more likely to be randomly located in the byte.

0xAE Port 1 Receive Synchronization Control

		Access / Notes	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7	RW	[no name]	Set to arm the receive and transmit sync triggers.
6	–	[no name]	Reserved.
5	RW	[no name]	Set to use DDR2 FIFO to transmit; clear to use DDR2 FIFO to receive.
4–3	–	[no name]	Reserved.
2	RW	[no name]	Set to disable the frame align requirement for on the receive sync trigger.
1–0	RW	[no name]	Set to select trigger source. 00 = trigger from port 1.

0xAF Port 1 Transmit Synchronization Control [Reserved]

0xB0–BF Port 1 [Reserved]

0xC0–DF Port 2 [See 0xA0–BF]

0xE0–FF Not Port-Specific

0xE0 Mezzanine FPGA Configuration File Version String

		Access / Notes	8-bit read-write / [no name]
			Use this register to read the FPGA configuration file version string from ROM. Write the ROM address to the register and read the ASCII data from the same register. The version string is a maximum of 64 bytes long, so only the first six bits of the address are significant.
Bit	**Access**	**Name**	**Description**
7–0	RW	ID_ADD_DATA	Write an address to read contents of flash memory. Result is... *bitfileName version.revision mm/dd/yyyy*
			The date given is the date the FPGA configuration file was created. Replace placeholders in italics with actual values — for example, `threep_10g_sdh_sdh 1.0 08/25/2010.`

0xE1 Mezzanine FPGA Configuration File Organization

		Access / Notes	8-bit read-only / [no name]
Bit	**Access**	**Name**	**Description**
7–0	R only	[no name]	A byte specifying the organization that created the FPGA configuration file currently loaded in the FPGA on the mezzanine board. An FPGA configuration file produced by EDT returns the value 0xFF.

0xE2–E3 Mezzanine FPGA Configuration File Design ID

		Access / Notes	16-bit read-only / [no name]
			This sixteen-bit number, assigned by the organization that created the FPGA configuration file as a file design ID, is loaded on the mezzanine board FPGA.
Bit	**Access**	**Name**	**Description**
15–0	R only	[no name]	For `threep_10g_sdh_sdh.bit,` the design ID is 0x1300.
			For `threep_10g_1g_1g.bit,` the design ID is 0x1301.
			For `threep_10g_emac_emac.bit,` the design ID is 0x1302.
			For `threep_stm64_sdh_sdh.bit,` the design ID is 0x1303.

0xE4–E6 DDR2 Bank Status and Control

		Access / Notes	8-bit read-write:
			0xE4 = THREEP_BANK0A_CTRL 0xE5 = THREEP_BANK0B_CTRL 0xE6 = THREEP_BANK1_CTRL
			If Bank 0A and Bank 0B are combined (as they are in the default FPGA configuration files – i.e., those with prefixes `threep_10g` and `threep_stm64`), then only Bank 0A is valid.
Bit	**Access**	**Name**	**Description**
7	–	[no name]	Reserved.
6	R only	PHY_INITDONE	DDR2 interface is trained.
5	R only	PLL_LOCK	Bank DDR2 interface clocks are ready.
4	R only	IDLY_RDY	IOdelay controller is ready.
3–1	–	[no name]	Reserved.
0	RW	PHY_RST	Set to reset DDR2 interface; clear to use DDR2.

0xE7 Serial Master Interface Status

		Access / Notes	8-bit read-write / THREEP_SER_MASTER_DEV_ADDR

Bit	Access	Name	Description
7	R only	SER_DEV_BSY	Read only. When set, the serial master is busy.
6	R only	SER_DEV_ACK_FAIL	Read only. When set, the serial slave failed to respond to the last command.
5–0	RW	SER_DEV_ADDR	Device 0 = SI5326: Ch0 transmit reference clock jitter attenuator Device 1 = SI570: Ch0 reference clock (transmit and receive) Device 2 = SI570: Ch1 reference clock Device 3 = SI570: Ch2 reference clock Device 4 = SFP+ EEPROM: Ch0 Device 5 = SFP+ diagnostic: Ch0 Device 6 = SFP+ EEPROM: Ch1 Device 7 = SFP+ diagnostic: Ch1 Device 8 = SFP+ EEPROM: Ch2 Device 9 = SFP+ diagnostic: Ch2 Device 10 = AMCC S19250: Ch0 LIU Device 11 = SFP ethernet PHY (electrical ethernet SFP only): Ch0 Device 12 = SFP ethernet PHY (electrical ethernet SFP only): Ch1 Device 13 = SFP ethernet PHY (electrical ethernet SFP only): Ch2

0xE8 Serial Master Interface Read

Access / Notes 8-bit read-write / THREEP_SER_MASTER_RD

Bit	Access	Name	Description
7–0	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the data returned from address.

0xE9 Serial Master Interface Register Address

Access / Notes 8-bit read-write / THREEP_SER_MASTER_REG_ADDR

Bit	Access	Name	Description
7–0	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the previously accessed serial slave register address.

0xEA Serial Master Interface Write

Access / Notes 8-bit read-write / THREEP_SER_MASTER_WR

Bit	Access	Name	Description
7–0	RW	[no name]	Write data to the register address in register 0xE9.

0xEB–ED Time Distribution

Access / Notes Three 8-bit registers (for Time Distribution user's guide, see Related Resources on page 11):

0xEB on the 3P = 0x60 on the Time Distribution board.
0xEC on the 3P = 0x61 on the Time Distribution board.
0xED on the 3P = 0x62 on the Time Distribution board.

0xEE PRBS Mode

		Access / Notes	8-bit read-write / THREEP_PRBS_MODE
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Sets mode for all internal mezzanine PRBS generators and checkers.

0xF4 Frequency Counter Control

		Access / Notes	8-bit read-write / THREEP_FREQ_CNT_EN
Bit	**Access**	**Name**	**Description**
7–4	RW	[no name]	Selects the frequency counter for readback from 0xF5–F7 Frequency Counter Value. 0 = Port 0 receive clock 1 = Port 1 receive clock 2 = Port 2 receive clock 3 = Port 0 transmit clock 4 = Port 1 transmit clock 5 = Port 2 transmit clock
3–0	RW	[no name]	Set to enable port frequency counters.

0xF5–F7 Frequency Counter Value

		Access / Notes	24-bit read-only / THREEP_FREQ_CNT
Bit	**Access**	**Name**	**Description**
23–0	R	[no name]	Reads the frequency counter value, as selected in bits 7–4 of 0xF4 Frequency Counter Control.

threep_stm64_sdh_sdh.bit – Extended Registers

0x800000–FF Port 0

0x800001–02 Port 0 Transmit Test Pattern

		Access / Notes	16-bit read-write / THREEP_P0_XMIT_PATTERN
Bit	**Access**	**Name**	**Description**
15–0	–	[no name]	Set the transmit test pattern.

0x800005–07 Port 0 B1 Error Count

		Access / Notes	24-bit read-only: 0x800005–07 (port 0) = THREEP_P0_B1_ERROR_CNT 0x800105–07 (port 1) = THREEP_P1_B1_ERROR_CNT 0x800205–07 (port 2) = THREEP_P2_B1_ERROR_CNT Controlled by registers 0x8B, AB, CB (for ports 0, 1, and 2, respectively) on page 36.
Bit	**Access**	**Name**	**Description**
23–0	R only	[no name]	The number of B1 bits found to be in error since the counter was last reset.

0x800008–0B Port 0 B2 Error Count

		Access / Notes	32-bit read-only: 0x800008–0B (port 0) = THREEP_P0_B2_ERROR_CNT 0x800108–0B (port 1) = THREEP_P1_B2_ERROR_CNT 0x800208–0B (port 2) = THREEP_P2_B2_ERROR_CNT Controlled by registers 0x8B, AB, CB (for ports 0, 1, and 2, respectively) on page 36.
Bit	**Access**	**Name**	**Description**
31–0	R only	[no name]	The number of B2 bits found to be in error since the counter was last reset.

0x80000C–0E Port 0 M1 Error Count

		Access / Notes	24-bit read-only: 0x80000C–0E (port 0) = THREEP_P0_M1_ERROR_CNT 0x80010C–0E (port 1) = THREEP_P1_M1_ERROR_CNT 0x80020C–0E (port 2) = THREEP_P2_M1_ERROR_CNT Controlled by registers 0x8B, AB, CB (for ports 0, 1, and 2, respectively) on page 36.
Bit	**Access**	**Name**	**Description**
23–0	R only	[no name]	The number of M1 bits found to be in error since the counter was last reset. The M1 byte is sent from the remote receiver of the signal, if that remote receiver has detected a B1 error. In that case, the B1 error mask is copied and sent back as the M1 byte.

0x80000F–10 Port 0 Loss of Frame Count

Access / Notes 16-bit read-only:

0x80000F–10 (port 0) = THREEP_P0_LOF_CNT
0x80010F–10 (port 1) = THREEP_P1_LOF_CNT
0x80020F–10 (port 2) = THREEP_P2_LOF_CNT

Controlled by registers 0x8B, AB, CB (for ports 0, 1, and 2, respectively) on page 36.

Bit	Access	Name	Description
15–0	R only	[no name]	The number of times framing was lost since the counter was last reset. This number equals the number of times that the LOCKED bit or the FRAMED bit has gone clear (bit 7 in 0xA8 Port 1 Receive Frame Status or bit 0 in 0xA7 Port 1 Receive Status). Framing is lost when four consecutive bad framing patterns are detected.

0x800011–12 Port 0 Frame Pattern Error Count

Access / Notes 16-bit read-only:

0x800011–12 (port 0) = THREEP_P0_FRM_PAT_CNT
0x800111–12 (port 1) = THREEP_P1_FRM_PAT_CNT
0x800211–12 (port 2) = THREEP_P2_FRM_PAT_CNT

Controlled by registers 0x8B, AB, CB (for ports 0, 1, and 2, respectively) on page 36.

Bit	Access	Name	Description
15–0	R only	[no name]	The number of times that the framing pattern was not correct, after data has been in frame. Because framing is not lost until the framing pattern has been incorrect four consecutive times, an incorrect framing pattern does not necessarily mean that framing was lost.

0x800013–14 Port 0 False Frame Count

Access / Notes 16-bit read-only:

0x800013–14 (port 0) = THREEP_P0_FALSE_FRM_CNT
0x800113–14 (port 1) = THREEP_P1_FALSE_FRM_CNT
0x800213–14 (port 2) = THREEP_P2_FALSE_FRM_CNT

Controlled by registers 0x8B, AB, CB (for ports 0, 1, and 2, respectively) on page 36.

Bit	Access	Name	Description
15–0	R only	[no name]	When searching for frame, the number of times that a possible frame pattern was detected but the signal was not framed. This can be useful for distinguishing whether the signal sometimes appears to be framed, or whether it always appears to be unframed, and therefore possibly gibberish.

0x800015–17 Port 0 Demux Bitmask

Access / Notes Three registers, each 8-bit read-write, with access names as specified below.

This register space addresses a 192-bit mask register that is divided into twelve 16-bit writes and can be 16 bits at a time. The lower four bits of 0x800017 address the desired 16-bit mask register, while the sixteen bits at 0x800015 and 0x800016 are the value written.

Bit 15 of address 0 disables the first byte of each 192-byte OC192/STM64 multiplexed group, and bit 0 of address 0x0B disables the last byte of each multiplexed group. To enable all bytes of the group, all bits are zero (the default).

NOTE: Bit 7 of register 0x800017 must be set to write, and clear to read.

For example, to enable STM1-(1,1,0) using pdb, write:

>>pdb -u *unit number*

: iw 800015 FF
: iw 800016 7F
: iw 800017 80
: iw 800015 FF
: iw 800016 FF
: iw 800017 81
: iw 800017 82
: iw 800017 83
: iw 800017 84
: iw 800017 82
: iw 800017 85
: iw 800017 86
: iw 800017 87
: iw 800017 88
: iw 800017 89
: iw 800017 8A
: iw 800017 8B

For register address 0x800015: Access = THREEP_P0_DEMUX_BITMASK_LO

Bit	Access	Name	Description
7–0		DEMUX_ MASK[7–0]	A bit pattern. A value of 1 masks the corresponding byte of each 192-byte multiplexed group.

For register address 0x800016: Access = THREEP_P0_DEMUX_BITMASK_HI

Bit		Name	Description
7–0		DEMUX_ MASK[15–8]	A bit pattern. A value of 1 masks the corresponding byte of each 192-byte multiplexed group.

For register address 0x800017: Access = THREEP_P0_DEMUX_MASK_ADDR

Bit	Access	Name	Description
7		WRITE_STROBE	A bit pattern. A value of 1 masks the corresponding byte of each 192-byte multiplexed group.
6–4		[no name]	A value of one to write and zero to read.
3–0		MASK_ADDR	Bitmask register address 0x00–0x0B.

0x800018–19 Port 0 Demux Bitmask Readback

Access / Notes Two registers, each 8-bit read-only / THREEP_P0_DEMUX_BITMASK_RD

Use this register space to read back the demultiplexing bitmask. To do so, write register 0x800017 with bit 7 clear to zero. Read the stored bit pattern in these two registers.

Bit	Access	Name	Description
7–0		[see next column]	A bit pattern. A value of 1 masks the corresponding byte of each 192-byte multiplexed group. For 0x800015, the name is: DEMUX_MASK_READ[7–0]. For 0x800016, the name is: DEMUX_MASK_READ[15–8].

0x800100–FF Port 1

0x800100 Port 1 Transmit National Byte

		Access / Notes	8-bit read-write: 0x800100 (port 1) = THREEP_P1_XMT_NATIONAL 0x800200 (port 2) = THREEP_P2_XMT_NATIONAL
Bit	**Access**	**Name**	**Description**
7–0	RW	NAT_BYTE	Define byte to be sent in the National Byte field of the frame.

0x800101–04 Port 1 Transmit Test Data

		Access / Notes	32-bit read-write (each access code addresses all 32 bits): 0x800101–04 (port 1) = THREEP_P1_XMT_TEST_DATA 0x800201–04 (port 2) = THREEP_P2_XMT_TEST_DATA
Bit	**Access**	**Name**	**Description**
31–0	RW	TEST_DATA	Bytes of a 32-bit transmit data test pattern.

0x800105–14 Port 1 [See 0x800005–14 Port 0]

0x800115 Port 1 Demux Bitmap

Access / Notes 8-bit read-write:

0x800115 (port 1) = THREEP_P1_DEMUX_BITMAP
0x800215 (port 2) = THREEP_P2_DEMUX_BITMAP

This register addresses a 48-bit mask register that is accessed via twelve 4-bit writes. The top four bits address the desired 4 bits of the mask register, while the bottom four bits are the value written.

Bit 3 of address 0 disables the first byte of each 48-byte OC48/STM16 multiplexed group, and bit 0 of address B disables the last byte of each multiplexed group. To enable all bytes of the group, all bits are 0 (the default).

Bit	Access	Name	Description
7–4	RW	MASK_ADDR	Bit register address 0x00–0B.
3–0	RW	DEMUX_MASK	Bitmask. A value of 1 masks the corresponding byte of each 48-byte multiplexed group.

STM1
enabling AU-3(1)

The mask is written 4 bits at a time; only bits 3–1 of the mask are used.

Example: To select AU-3(1), the first AU-3, use the `pdb` command...

```
: iw 800115 07
```

STM4
enabling STM1(1,0)

The mask is written 4 bits at a time; only the first 12 bits of the mask are used.

Example: To select AU-4(1,0), the first STM1, use the `pdb` commands...

```
: iw 800115 07
: iw 800115 17
: iw 800115 27
```

STM16
enabling STM1(1,1,0)

The mask is written 4 bits at a time; only the first 48 bits of the mask are used.

Example: To select AU-4(1,1,0), the first STM1, use the `pdb` commands...

```
: iw 800115 07
: iw 800115 1F
: iw 800115 2F
: iw 800115 3F
: iw 800115 47
: iw 800115 5F
: iw 800115 6F
: iw 800115 7F
: iw 800115 87
: iw 800115 9F
: iw 800115 AF
: iw 800115 BF
```

0x800116 Port 1 Demux Bitmap Readback

Access / Notes 8-bit read-write:

0x800116 (port 1) = THREEP_P1_DEMUX_BITMAP_READ
0x800216 (port 2) = THREEP_P2_DEMUX_BITMAP_READ

Reads back the demultiplexing bitmask. Write this register with the address of the 4-bit mask you wish to read. Read the stored bit pattern in the bottom four bits.

Bit	Access	Name	Description
7–4	RW	MASK_ADDR	Bit register address 0x00 – 0x0B.
3–0	RW	DEMUX_MASK	The bitmask. A value of 1 masks the corresponding byte of each 48-byte multiplexed group.

0x800200–FF Port 2 [See 0x800100–FF]

threep_sdh_sdh_sync.bit – Standard Registers

0x00–7F [See threep.bit]

0x80–9F Port 0

0x80–8E Port 0 [Reserved]

0x8F Port 0 Transmit Synchronization Control

		Access / Notes	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7–6	–	[no name]	Reserved.
5	RW	[no name]	Set to initiate synchronization of capture and/or transmit on ports 1 and 2.
4–0	–	[no name]	Reserved.

0x90–9F Port 0 [Reserved]

0xA0–BF Port 1

0xA0 Port 1 Configuration 0

		Access / Notes	8-bit read-write (sets options in the SDH LIU): 0xA0 (port 1) = THREEP_P1_CONFIG0 0xC0 (port 2) = THREEP_P2_CONFIG0
Bit	**Access**	**Name**	**Description**
7	RW	PRBS_EN	When set, the LIU transmits a full-band PRBS7 code. The LIU receiver checks the code and sets a bit in 0xA2 Port 1 Status.
6	RW	LOCAL_LOOP	Sets local loopback. The port receiver is connected directly to the corresponding port transmitter.
5	RW	REMOTE_LOOP	Sets remote loopback. Data received through the fiberoptic connector is immediately transmitted out the corresponding transmit connector. The received data is also forwarded for DMA, if DMA is enabled.

4	RW	AUTO_DETECT	When this bit is set and bits 3-2 (RX_SEL) are 00, the LIU automatically detects the incoming bit rate and reports the results in 0xA2 Port 1 Status. Texas Instruments does not recommend using automatic detection.
3–2	RW	RX_SEL	Set the expected receive bit rate as follows: 00 = OC48/STM16 01 = Gigabit ethernet 10 = OC12/STM4 11 = OC3/STM1
1	RW	LOCK_REF	When set, the LIU receive clock is locked to the transmit clock internal to the LIU. For normal operation, keep this bit clear.
0	–	[no name]	Reserved.

0xA1 Port 1 Configuration 1

		Access / Notes	8-bit read-write: 0xA1 (port 1) = THREEP_P1_CONFIG1 0xC1 (port 2) = THREEP_P2_CONFIG1 Sets options in the SDH LIU; see link under Related Resources on page 11.
Bit	**Access**	**Name**	**Description**
7–5	–	[no name]	Reserved.
4	RW	LOOPTIME	Set this bit to obtain transmit timing from the receive timing. Normal 3P operation is 0 (internal timing).
3–2	RW	PRE2511	The de-emphasis level of the SDH LIU electrical interface can be programmed. For 3P operation, always set to 00.
1–0	RW	CONFG2511	The SDH LIU can be configured as follows: 00 = Full duplex transceiver, required for normal operation 01 = Transmit only 10 = Receive only 11 = Repeater mode For 3P operation, always set to 00 — full duplex transceiver.

0xA2 Port 1 Status

		Access / Notes	8-bit read-only: 0xA2 (port 1) = THREEP_P1_STATUS 0xC2 (port 2) = THREEP_P2_STATUS Sets options in the SDH LIU; see link under Related Resources on page 11.
Bit	**Access**	**Name**	**Description**
7	R only	SIG_DET	Set when the SFP transceiver module has detected an incoming signal.
6	–	[no name]	Reserved; reads 0.
5	R only	LOL	Set when the receive phase-locked loop cannot lock to the incoming data.

4	R only	LOS	Set when the SDH LIU detects loss of signal. This bit is not reset until a SONET or SDH frame is detected.
3–2	R only	RATE_DET	Bits set to the RX rate detected. Set for bit rates as follows: 00 = OC48/STM16 01 = Gigabit ethernet 10 = OC12/STM4 11 = OC3/STM1
1	R only	PRBSPASS	The receiver is receiving a valid full-band PRBS7 code as transmitted by the SDH LIU , when PRBS mode is enabled; see bit 7 (PRBS_EN) of 0xA0 Port 1 Configuration 0. The PRBS mode must be enabled, although the code can come from any source. **NOTE:** Certain bit error testers use inverted PRBS7 code.
0	R only	SPILL2511	SDH LIU transmit FIFO overflow. This can occur in loop-timing mode only if the internal transmit data clock is not the same as the received bit rate.

0xA3–A4 Port 1 [See 0x83–84]

0xA5 Port 1 Receive Framing Control

		Access / Notes	8-bit read-write: 0xA5 (port 1) = THREEP_P1_RCV_FRAMING 0xC5 (port 2) = THREEP_P2_RCV_FRAMING
Bit	**Access**	**Name**	**Description**
7	–	[no name]	Reserved.
6	RW	EN_PAR_CNT	Set to enable count of parity errors; clear to reset the counter.
5	RW	SUSPEND_AQ	Set to halt data acquisition if FIFO overflow occurs.
4	RW	DISABLE_SCRAM	Set to disable descrambling on received framed data. You must set bit 0 (FRAME_EN) and be in frame before this bit has any effect.
	RW	DISABLE_8B10B	For ethernet bit files only: Set to disable the 8b/10b decoder (see Framing on page 20).
3–2	RW	RX_DATA_SRC	00 disables the 512 MB onboard FIFO 01 enables the 512 MB onboard FIFO 1*x* test mode
1	RW	FRAME_EN	Set to allow data acquisition only when the framer is locked to the incoming signal. Collected data is also descrambled.
	RW	MAC_FILTER	Clear to acquire raw data without framing or descrambling. For ethernet bit files only: Set to align data. See also Framing on page 20.
0	RW	RESET_FRM	Set, then clear to cause the framing circuits to drop and then relock onto the framing pattern.

0xA6 Port 1 Receive Filter Control

		Access / Notes	8-bit read-write: 0x86 (port 1) = THREEP_P1_RCV_FILTER 0xC6 (port 2) = THREEP_P2_RCV_FILTER
Bit	**Access**	**Name**	**Description**
7–4	–	[no name]	Reserved.
3	RW	FORCE_ALL_DATA	For ethernet bit files only: Set to force all idles and other command symbols. See also Framing on page 20.
2–1	–	[no name]	Reserved.
0	RW	OVERHEAD_ONLY	Set to acquire SONET / SDH frame overhead only; the payload is discarded.

0xA7 Port 1 Receive Status

		Access / Notes	8-bit read-only: 0xA7 (port 1) = THREEP_P1_RCV_STATUS 0xC7 (port 2) = THREEP_P2_RCV_STATUS
Bit	**Access**	**Name**	**Description**
7–1	–	[no name]	Reserved; always reads 0.
0	R only	FRAMED	Set when incoming data is framed.

0xA8 Port 1 Receive Frame Status

Access / Notes 8-bit read-only:

0xA8 (port 1) = THREEP_P1_RCV_FRAME_STATUS
0xC8 (port 2) = THREEP_P2_RCV_FRAME_STATUS

Bit	Access	Name	Description
7	R only	LOCKED	Set when frame is locked – same as bit 0 (FRAMED) in 0xA7 Port 1 Receive Status.
6	R only	FOUND	Set when frame pattern is found.
5–4	R only	DROP_CNT	The number of pattern mismatches in framer state machine.
3–2	R only	MATCH_CNT	The number of pattern matches in framer state machine.
1	R only	BYTE_SYNC	Set when the byte synchronization framing pattern is found.
0	R only	BIT_SYNC	Set when the bit synchronization framing pattern is found.

0xA9 Port 1 Transmit Framing Configuration

Access / Notes 8-bit read-write / [no name]:

0xA9 (port 1) = THREEP_P1_XMT_FRAMING
0xC9 (port 2) = THREEP_P2_XMT_FRAMING

Bits 7 and 6 work in conjunction with 0xA0 Port 1 Configuration 0, bits 3 and 2, to set up the framer.

Bit	Access	Name	Description
7–6	RW	[no name]	11 = OTU1 (when 0xA0 Port 1 Configuration 0 bits 3 and 2 = 00). 01 = STM*x* (when 0xA0 Port 1 Configuration 0 bits 3 and 2 have set *x* to be 1/4/16)
5	RW	[no name]	Set to initiate the transmit of the sync signal trigger.
4	–	[no name]	Reserved.
3	RW	EN_SCRAMBLE	Set to enable scrambling of output data if an OC / STM frame is detected.
2	RW	TX_FRAME_EN	Set to enable local framing with BIP error feedback. Data from the PCI bus is payload only and aligned with the AU pointer 0.
1	RW	TEST_DATA	Set to send test data; clear for normal operation.
0	RW	RESET_PTR	Toggle high, then low, to send the AU pointer reset command.

0xAA Port 1 Transmit Status

Access / Notes 8-bit read-only:

0xAA (port 1) = THREEP_P1_TX_STATUS
0xCA (port 2) = THREEP_P2_TX_STATUS

Bit	Access	Name	Description
7–1	–	[no name]	Reserved (may not always read 0).
0	R only	TX_FRAMED	Set when a frame is detected in transmitted data. If scrambling is enabled in bit 3 of 0xA9 Port 1 Transmit Framing Configuration, then the data is being scrambled.

0xAB Port 1 [See 0x8B]

0xAC Port 1 B1 Error Mask

Access / Notes 8-bit read-only:

0xAB (port 1) = THREEP_P1_B1_ERROR_MASK
0xCB (port 2) = THREEP_P2_B2_ERROR_MASK

Bit	Access	Name	Description
7–0	R only	[no name]	The value of the error mask for the last B1 error. A B1 error mask is one byte resulting from a logical operation on the previous frame. Errors occurring regularly in the same bit of the byte can indicate a problem in the sender's or receiver's equipment. If errors are occurring on the fiber, the B1bits in error are more likely to be randomly located in the byte.

0xAE Port 1 Receive Synchronization Control

Access / Notes 8-bit read-write / [no name]

0xAE (port 1)
0xCE (port 2)

Bit	Access	Name	Description
7	RW	[no name]	Set to arm the receive and transmit sync triggers.
6	–	[no name]	Reserved.
5	RW	[no name]	Set to use DDR2 FIFO to transmit; clear to use DDR2 FIFO to receive.
4–3	–	[no name]	Reserved.
2	RW	[no name]	Set to disable the frame align requirement for on the receive sync trigger.
1–0	RW	[no name]	Set to select trigger source. 00 = trigger from port 0.

0xAF Port 1 Transmit Synchronization Control [Reserved]

0xC0–DF Port 2 [See 0xA0–BF]

0xE0–FF Not Port-Specific

0xE0 Mezzanine FPGA Configuration File Version String

Access / Notes 8-bit read-write / [no name]

Use this register to read the FPGA configuration file version string from ROM. Write the ROM address to the register and read the ASCII data from the same register. The version string is a maximum of 64 bytes long, so only the first six bits of the address are significant.

Bit	Access	Name	Description
7–0	RW	ID_ADD_DATA	Write an address to read contents of flash memory. Result is... *bitfileName version.revision mm/dd/yyyy* The date given is the date the FPGA configuration file was created. Replace placeholders in italics with actual values — for example, `threep_10g_sdh_sdh 1.0 08/25/2010.`

0xE1 Mezzanine FPGA Configuration File Organization

Access / Notes 8-bit read-only / [no name]

Bit	Access	Name	Description
7–0	R only	[no name]	A byte specifying the organization that created the FPGA configuration file currently loaded in the FPGA on the mezzanine board. An FPGA configuration file produced by EDT returns the value 0xFF.

0xE2–E3 Mezzanine FPGA Configuration File Design ID

Access / Notes 16-bit read-only / [no name]

This sixteen-bit number, assigned by the organization that created the FPGA configuration file as a file design ID, is loaded on the mezzanine board FPGA.

Bit	Access	Name	Description
15–0	R only	[no name]	For `threep_10g_sdh_sdh.bit,` the design ID is 0x1300. For `threep_10g_1g_1g.bit,` the design ID is 0x1301. For `threep_10g_emac_emac.bit,` the design ID is 0x1302. For `threep_stm64_sdh_sdh.bit,` the design ID is 0x1303.

0xE4–E6 DDR2 Bank Status and Control

Access / Notes 8-bit read-write:

0xE4 = THREEP_BANK0A_CTRL
0xE5 = THREEP_BANK0B_CTRL
0xE6 = THREEP_BANK1_CTRL

If Bank 0A and Bank 0B are combined (as they are in the default FPGA configuration files – i.e., those with prefixes `threep_10g` and `threep_stm64`), then only Bank 0A is valid.

Bit	Access	Name	Description
7	–	[no name]	Reserved.
6	R only	PHY_INITDONE	DDR2 interface is trained.
5	R only	PLL_LOCK	Bank DDR2 interface clocks are ready.
4	R only	IDLY_RDY	IOdelay controller is ready.
3–1	–	[no name]	Reserved.
0	RW	PHY_RST	Set to reset DDR2 interface; clear to use DDR2.

0xE7 Serial Master Interface Status

Access / Notes 8-bit read-write / THREEP_SER_MASTER_DEV_ADDR

Bit	Access	Name	Description
7	R only	SER_DEV_BSY	Read only. When set, the serial master is busy.
6	R only	SER_DEV_ACK_ FAIL	Read only. When set, the serial slave failed to respond to the last command.
5–0	RW	SER_DEV_ADDR	Device 0 = SI5326: Ch0 transmit reference clock jitter attenuator Device 1 = SI570: Ch0 reference clock (transmit and receive) Device 2 = SI570: Ch1 reference clock Device 3 = SI570: Ch2 reference clock Device 4 = SFP+ EEPROM: Ch0 Device 5 = SFP+ diagnostic: Ch0 Device 6 = SFP+ EEPROM: Ch1 Device 7 = SFP+ diagnostic: Ch1 Device 8 = SFP+ EEPROM: Ch2 Device 9 = SFP+ diagnostic: Ch2 Device 10 = AMCC S19250: Ch0 LIU Device 11 = SFP ethernet PHY (electrical ethernet SFP only): Ch0 Device 12 = SFP ethernet PHY (electrical ethernet SFP only): Ch1 Device 13 = SFP ethernet PHY (electrical ethernet SFP only): Ch2

0xE8 Serial Master Interface Read

Access / Notes 8-bit read-write / THREEP_SER_MASTER_RD

Bit	Access	Name	Description
7–0	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the data returned from address.

0xE9 Serial Master Interface Register Address

		Access / Notes	8-bit read-write / THREEP_SER_MASTER_REG_ADDR
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Write the register address on the serial slave that you wish to read. Read the previously accessed serial slave register address.

0xEA Serial Master Interface Write

		Access / Notes	8-bit read-write / THREEP_SER_MASTER_WR
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Write data to the register address in register 0xE9.

0xEB–ED Time Distribution

		Access / Notes	Three 8-bit registers (for Time Distribution user's guide, see Related Resources on page 11): 0xEB on the 3P = 0x60 on the Time Distribution board. 0xEC on the 3P = 0x61 on the Time Distribution board. 0xED on the 3P = 0x62 on the Time Distribution board.

0xEE PRBS Mode

		Access / Notes	8-bit read-write / THREEP_PRBS_MODE
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	Sets mode for all internal mezzanine PRBS generators and checkers.

0xF4 Frequency Counter Control

		Access / Notes	8-bit read-write / THREEP_FREQ_CNT_EN
Bit	**Access**	**Name**	**Description**
7–4	RW	[no name]	Selects the frequency counter for readback from 0xF5–F7 Frequency Counter Value. 0 = Port 0 receive clock 1 = Port 1 receive clock 2 = Port 2 receive clock 3 = Port 0 transmit clock 4 = Port 1 transmit clock 5 = Port 2 transmit clock
3–0	RW	[no name]	Set to enable port frequency counters.

0xF5–F7 Frequency Counter Value

		Access / Notes	24-bit read-only / THREEP_FREQ_CNT
Bit	**Access**	**Name**	**Description**
23–0	R	[no name]	Reads the frequency counter value, as selected in bits 7–4 of 0xF4 Frequency Counter Control.

threep_sdh_sdh_sync.bit – Extended Registers

0x800000–FF Port 0 [Reserved]

0x800100–FF Port 1

0x800100 Port 1 Transmit National Byte

		Access / Notes	8-bit read-write: 0x800100 (port 1) = THREEP_P1_XMT_NATIONAL 0x800200 (port 2) = THREEP_P2_XMT_NATIONAL
Bit	**Access**	**Name**	**Description**
7–0	RW	NAT_BYTE	Define byte to be sent in the National Byte field of the frame.

0x800101–04 Port 1 Transmit Test Data

		Access / Notes	32-bit read-write (each access code addresses all 32 bits): 0x800101–04 (port 1) = THREEP_P1_XMT_TEST_DATA 0x800201–04 (port 2) = THREEP_P2_XMT_TEST_DATA
Bit	**Access**	**Name**	**Description**
31–0	RW	TEST_DATA	Bytes of a 32-bit transmit data test pattern.

0x800105–07 Port 1 B1 Error Count

		Access / Notes	24-bit read-only: 0x800105–07 (port 1) = THREEP_P1_B1_ERROR_CNT 0x800205–07 (port 2) = THREEP_P2_B1_ERROR_CNT Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.
Bit	**Access**	**Name**	**Description**
23–0	R only	[no name]	The number of B1 bits found to be in error since the counter was last reset.

0x800108–0B Port 1 B2 Error Count

Access / Notes 32-bit read-only:

0x800108–0B (port 1) = THREEP_P1_B2_ERROR_CNT
0x800208–0B (port 2) = THREEP_P2_B2_ERROR_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
31–0	R only	[no name]	The number of B2 bits found to be in error since the counter was last reset.

0x80010C–0E Port 1 M1 Error Count

Access / Notes 24-bit read-only:

0x80010C–0E (port 1) = THREEP_P1_M1_ERROR_CNT
0x80020C–0E (port 2) = THREEP_P2_M1_ERROR_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
23–0	R only	[no name]	The number of M1 bits found to be in error since the counter was last reset. The M1 byte is sent from the remote receiver of the signal, if that remote receiver has detected a B1 error. In that case, the B1 error mask is copied and sent back as the M1 byte.

0x80010F–10 Port 1 Loss of Frame Count

Access / Notes 16-bit read-only:

0x80010F–10 (port 1) = THREEP_P1_LOF_CNT
0x80020F–10 (port 2) = THREEP_P2_LOF_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
15–0	R only	[no name]	The number of times framing was lost since the counter was last reset. This equals the number of times that the LOCKED bit or the FRAMED bit has gone clear (bit 7 in 0xA8 Port 1 Receive Frame Status or bit 0 in 0xA7 Port 1 Receive Status). Framing is lost when four consecutive bad framing patterns are detected.

0x800111–12 Port 1 Frame Pattern Error Count

Access / Notes 16-bit read-only:

0x800111–12 (port 1) = THREEP_P1_FRM_PAT_CNT
0x800211–12 (port 2) = THREEP_P2_FRM_PAT_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
15–0	R only	[no name]	The number of times that the framing pattern was not correct, after data has been in frame. Because framing is not lost until the framing pattern has been incorrect four consecutive times, an incorrect framing pattern does not necessarily mean that framing was lost.

0x800113–14 Port 1 False Frame Count

Access / Notes 16-bit read-only:

0x800113–14 (port 1) = THREEP_P1_FALSE_FRM_CNT
0x800213–14 (port 2) = THREEP_P2_FALSE_FRM_CNT

Controlled by registers 0xAB, CB (for ports 1 and 2) on page 36.

Bit	Access	Name	Description
15–0	R only	[no name]	When searching for frame, the number of times that a possible frame pattern was detected but the signal was not framed. This can be useful for distinguishing whether the signal sometimes appears to be framed, or whether it always appears to be unframed, and therefore possibly gibberish.

0x800115 Port 1 Demux Bitmap

Access / Notes 8-bit read-write:

0x800115 (port 1) = THREEP_P1_DEMUX_BITMAP
0x800215 (port 2) = THREEP_P2_DEMUX_BITMAP

This register addresses a 48-bit mask register that is accessed via twelve 4-bit writes. The top four bits address the desired 4 bits of the mask register, while the bottom four bits are the value written.

Bit 3 of address 0 disables the first byte of each 48-byte OC48/STM16 multiplexed group, and bit 0 of address B disables the last byte of each multiplexed group. To enable all bytes of the group, all bits are 0 (the default).

Bit	Access	Name	Description
7–4	RW	MASK_ADDR	Bit register address 0x00–0B.
3–0	RW	DEMUX_MASK	Bitmask. A value of 1 masks the corresponding byte of each 48-byte multiplexed group.

STM1
enabling AU-3(1)

The mask is written 4 bits at a time; only bits 3–1 of the mask are used.

Example: To select AU-3(1), the first AU-3, use the `pdb` command...

: iw 800115 07

STM4
enabling STM1(1,0)

The mask is written 4 bits at a time; only the first 12 bits of the mask are used.

Example: To select AU-4(1,0), the first STM1, use the `pdb` commands...

: iw 800115 07
: iw 800115 17
: iw 800115 27

STM16
enabling STM1(1,1,0)

The mask is written 4 bits at a time; only the first 48 bits of the mask are used.

Example: To select AU-4(1,1,0), the first STM1, use the `pdb` commands...

: iw 800115 07
: iw 800115 1F
: iw 800115 2F
: iw 800115 3F
: iw 800115 47
: iw 800115 5F
: iw 800115 6F
: iw 800115 7F
: iw 800115 87
: iw 800115 9F
: iw 800115 AF
: iw 800115 BF

0x800116 Port 1 Demux Bitmap Readback

Access / Notes 8-bit read-write:

0x800116 (port 1) = THREEP_P1_DEMUX_BITMAP_READ
0x800216 (port 2) = THREEP_P2_DEMUX_BITMAP_READ

Reads back the demultiplexing bitmask. Write this register with the address of the 4-bit mask you wish to read. Read the stored bit pattern in the bottom four bits.

Bit	Access	Name	Description
7–4	RW	MASK_ADDR	Bit register address 0x00 – 0x0B.
3–0	RW	DEMUX_MASK	The bitmask. A value of 1 masks the corresponding byte of each 48-byte multiplexed group.

0x800200–FF Port 2

0x800200–16 Port 2 [See 0x800100–16 Port 1]

Revision Log

Below is a history of modifications to this guide.

Date	Rev	By	Pp	Detail
20131219	01	PH,SB, SC	All	Completed body content and registers.
20130913	01	PH,SB	85-86	0x800015-17 Port 0Demux Bitmask: Rearranged pdb commands from 3 columns to 1. 0x800115 Port 1 Demux Bitmap: Converted notes at top of register to list of pdb commands.
20111100	01	PH,SB	All	Removed references to Sun Solaris OS.
20110103	01	PH,SB	19-38	For duplicated registers, separated one combined title at the first hex location into distinct titles at all hex locations (i.e., “0x81, C1” becomes “0x81” and “0xC1”), with each title linking back to the first hex location.
20101229	00	PH,SB	All	Drafted new unpublished guide.