
The eclssd16 FPGA Configuration File

The `eclssd16.bit` FPGA configuration file is firmware intended for the UI Xilinx on the PCI SS/GS main board when used with the ECL mezzanine board. This document describes the connector pinout and registers that it defines. Information on the mezzanine board itself can be found in:

[PCI SS/GS ECL User's Guide](#)

www.edt.com/manuals/PCD/ecl.pdf

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Connector Pinouts

Table 1 describes the connection from the PCI SS/GS board to the connector, with the ECL mezzanine board, when loaded with with `eclssd16.bit`.

The board uses a high-density 68-pin SCSI-type I/O connector (Tyco part number 787169-7), with a straight-shielded backshell (Tyco part number 750752-1). You can use a typical SCSI cable (Tyco part number 749621-7) if your equipment has a SCSI connector.

NOTE Do not connect your own circuits to the unused pins, as they may be internally connected.

Table 1. ECL (eclssd16.bit) Connector Pinout

Pin	Signal	Pin	Signal
1	CH15CLK+	35	CH15CLK–
2	CH0D+	36	CH0D–
3	CH0CLK+	37	CH0CLK–
4	CH1D+	38	CH1D–
5	CH1CLK+	39	CH1CLK–
6	CH2D+	40	CH2D–
7	CH2CLK+	41	CH2CLK–
8	CH3D+	42	CH3D–
9	CH3CLK+	43	CH3CLK–
10	CH4D+	44	CH4D–
11	CH4CLK+	45	CH4CLK–
12	CH9CLK+	46	CH9CLK–
13	CH5D+	47	CH5D–
14	CH5CLK+	48	CH5CLK–
15	CH6D+	49	CH6D–
16	CH6CLK+	50	CH6CLK–
17	CH12CLK+	51	CH12CLK–
18	CH13D+	52	CH13D–
19	CH7D+	53	CH7D–
20	CH7CLK+	54	CH7CLK–
21	reserved	55	reserved
22	CH8D+	56	CH8D–
23	CH12D+	57	CH12D–
24	CH11CLK+	58	CH11CLK–
25	CH11D+	59	CH11D–
26	CH10CLK+	60	CH10CLK–
27	CH8CLK+	61	CH8CLK–
28	CH9D+	62	CH9D–
29	CH10D+	63	CH10D–
30	CH13CLK+	64	CH13CLK–
31	CH14D+	65	CH14D–
32	CH14CLK+	66	CH14CLK–
33	CH15D+	67	CH15D–
34	ground	68	ground

Registers

The following registers are implemented in the firmware `eclssd16.bit`.

Applications can access the ECL registers through the DMA library routines especially `edt_reg_read()` and `edt_reg_write()`, using the symbolic names listed under “Access” for each register.

The following registers are implemented but not used:

- Data Path (0x01)
- Function (0x02)
- Status (0x03)
- Status Polarity (0x04)
- Direction Control (0x06 and 0x07)
- PLL 0 Divider (0x24 and 0x25)
- PLL 2 Divider (0x28 and 0x29)
- PLL 3 Divider (0x2A and 0x2B)

Command Register

Size	8-bit
I/O	read-write
Address	0x00
Access	PCD_CMD

Bit	Name	Description
7	WORDFLUSH	When set, enables transfer of one word at a time. When clear, enables burst mode.
6–4		not used
3	CMD_EN	Set this bit, and enable the required channels in the Channel Enable Register , for DMA to occur. When clear, resets all channels, flushes the FIFOs, and clears all under- and overflow bits.
2–0		not used

Configuration Register

Size	8-bit
I/O	read-write
Address	0x0F
Access	PCD_CONFIG

Bit	Name	Description
7–4		not used
3	SSWAP	Swaps the order of the two 16-bit short words in one 32-bit data word, so that <i>short 2</i> is transferred before <i>short 1</i> . Does not change the order of the bits within each short. See Figure 1 for the details of data word structure..
2–1		not used
0	BSWAP	Swaps the order of bytes 1 and 2, and also bytes 3 and 4, in a 32-bit data word, so that the bytes are transferred in the order 2, 1, 4, 3. Does not change the order of the bits within each byte. See Figure 1 for the details of data word structure..

NOTE The [Least Significant Bit First Register](#) can also affect the order in which data is transferred.

[Figure 1](#) shows the structure of a 32-bit data word, with no swapping in effect. With SHORTSWAP set, short 0 appears before short 1. With BYTESWAP set, byte 2 appears before byte 3, and byte 0 before byte 1. With both set, byte 0 appears first, followed by byte 1, byte 2, and finally byte 3.

Figure 1. Data Word Structure

short 1																short 2															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
byte 1								byte 2								byte 3								byte 4							

Channel Enable Register

Size	16-bit
I/O	read-write
Address	0x10 and 0x11
Access	SSD16_CHEN

Bit	Name	Description
15–0	CH_ENABLE	A value of one in a bit enables the corresponding channel for DMA. Channels correspond to register bits as shown in Table 2 .

Table 2. How Channels Correspond to Bits in Registers

Register	register with low address								register with high address							
Bit number	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Channel number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Channel Direction Register

Size	16-bit
I/O	read-write
Address	0x12 and 0x13
Access	SSD16_CHDIR

Bit	Name	Description
15–0	CH_DIR	A value of zero in a bit enables input for the corresponding DMA channel; a value of one enables output. Channels correspond to register bits as shown in Table 2 .

Channel Edge Register

Size	16-bit
I/O	read-write
Address	0x14 and 0x15
Access	SSD16_CHEDGE

Bit	Name	Description
15–0	EDGE	For input channels, a value of one in a bit indicates that the corresponding channel latches data on the rising edge of its clock. a value of 0 indicates that it latches data on the falling edge. For output channels, a value of one indicates that a new bit is output on the rising edge, and a value of zero that it's output on the falling edge. Channels correspond to register bits as shown in Table 2.

Least Significant Bit First Register

Size	16-bit
I/O	read-write
Address	0x16 and 0x17
Access	SSD16_LSB

Bit	Name	Description
15–0	LSB_FIRST	When set for a channel, the least significant bit of each 8-bit data byte is the first bit, and the most significant bit is the last. When clear for a channel, the most significant bit of the byte is the first bit.

NOTE Byte Swap and Short Swap in the [Configuration Register](#) can also affect the order of bits in a 32-bit word. A combination of these bits allow the data to be formatted correctly for your host computer and application.

Underflow Register

Size	16-bit
I/O	read only
Address	0x18 and 0x19
Access	SSD16_UNDER

Bit	Name	Description
15–0	UNDERFLOW	A value of 1 in a bit indicates that the corresponding channel's internal FIFO has underflowed since the previous CMD_EN or CHANNEL_ENABLE. Reset by first disabling, then re-enabling, the channel (see the Channel Enable Register).

Overflow Register

Size	16-bit
I/O	read only
Address	0x1A and 0x1B
Access	SSD16_OVER

Bit	Name	Description
15–0	OVERFLOW	A value of 1 in a bit indicates that the corresponding channel's internal FIFO has overflowed since the previous CMD_EN or CHANNEL_ENABLE. Reset by first disabling, then re-enabling, the channel (see the Channel Enable Register).

Data Invert Register

Size	16-bit
I/O	read only
Address	0x1C and 0x1D
Access	SSD16_CHINVERT

Bit	Name	Description
15–0	CH_INVERT	A value of 1 in a bit indicates that the corresponding channel's data is inverted — a one becomes a zero, and vice-versa.

PLL Programming Register

Size	8-bit
I/O	read-write
Address	0x20
Access	EDT_SS_PLL_CTL
Comment	The program <code>set_ss_vco</code> uses this register to program the serial interface of the four PLLs.

Bit	Name	Description
7	PLL_SCLK	Connected to all four PLL serial clock inputs.
6	PLL_DATA	Connected to all four PLL serial data inputs.
5–4		not used
3–0	PLL_STROBE	Connected to the strobe inputs of PLL 3–0, respectively.

Clock Select Register

Size	8-bit
I/O	read-write
Address	0x21
Access	EDT_SS_CLK_SEL
Comment	Selects output clock timing source. The internal clock is the default. External clocks let you choose an input channel's clock to serve as the output transmit clock for all output channels.

Bit	Values (0x)	Description
7–0	00	Internal from PLL1
	01	External, channel 0 input clock
	02	External, channel 1 input clock
	03	External, channel 2 input clock
	04	External, channel 3 input clock
	05	External, channel 4 input clock
	06	External, channel 5 input clock
	07	External, channel 6 input clock
	08	External, channel 7 input clock
	09	External, channel 8 input clock
	0A	External, channel 9 input clock
	0B	External, channel 10 input clock
	0C	External, channel 11 input clock
	0D	External, channel 12 input clock
	0E	External, channel 13 input clock
	0F	External, channel 14 input clock
	10	External, channel 15 input clock
	20	reserved
	40	reserved

PRBS15 Generator Register

Size	8-bit
I/O	read-write
Address	0x22
Access	SSD16_PRBS15_EN

Bit	Description
7–0	Set any bit to generate PRBS15 test code out on all channels. Clear all bits to stop PRBS15 code generation.

PLL 1 Divider Register

Size	16-bit
I/O	read-write
Address	0x26 and 0x27
Access	EDT_SS_PLL1_CLK
Comment	This register is set by <code>set_ss_vco</code> .

Bit	Name	Description
15–0	PLL1_DIV	A post-scalar divider used to achieve lower frequencies than those at which the PLLs can be programmed. After this division (if any), the clocks are divided by two for an even duty cycle — half the time high, and half low. <code>set_ss_vco</code> takes this into account. PLL1 sets the output clock for the diagnostic PRBS15 test data generator.

Bit Error Control Register

Size	8-bit
I/O	read-write
Address	0x58
Access	SSD16_PRBS_ERR_CTRL
Comment	Used for testing.

Bit	Name	Description
7	RESET	Set to reset the PRBS15 test code generator.
6	ERROR	Set to insert an error in the PRBS15 pattern generated, for testing purposes.
5–0		not used

Board ID Register

Size	8-bit
I/O	read-write
Address	0x7F
Access	EDT_BOARDID
Comment	Returns a unique four-bit code corresponding to the mezzanine board installed. A value of 2 indicates an extended board ID. To read an extended board ID code, use the application <code>extbdid.exe</code> or the EDT DMA library routine <code>edt_get_boardID</code> .

Bit	Name	Description
7–5		used by <code>extbdid.exe</code>
4		not used; always set
3–0	BOARD_ID	The ID code of the installed mezzanine board: 12 3x3G 11 OC192 10 16TE3 - F Combo I/O, ECL - E Combo II I/O, RS-422 - D Combo III I/O, ECL - C Combo III I/O, LVDS - B Combo III I/O, RS-422 - A SRXL (with Graychips) 9 TLK1501 I/O 8 ECL I/O 7 Combo II I/O, LVDS 6 OCM 5 HRC for E4, STM-1, OC3 4–2 reserved 1 LVDS I/O 0 RS-422 I/O