Addendum: Test Procedures – ssloptest and xtest

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Test Procedures: sslooptest and xtest

Overview

This document describes procedures for using the EDT loopback test programs `sslooptest` and `xtest`. These programs, along with their C source, are included in your EDT installation package.

Applicable Boards

Table 1 lists the EDT boards which can be tested with `sslooptest` and `xtest`.

Table 1. Boards tested with `sslooptest` and `xtest`

Use sslooptest to test these boards*	Use xtest to test these boards*
• A PCI CDa board using the FPGA configuration file `cda16.bit` for 16-channel DMA operation. • A PCI SS, PCI GS, or PCIe8 LX / FX / SX main board using an EDT FPGA configuration file for multichannel operation, along with almost any EDT mezzanine board paired with it.	• A PCI CDa board using the FPGA configuration file `cda1.bit` for 1-channel DMA operation. • Any PCI CD-20 or PCI CD-60 board.

* If you run `sslooptest` and it detects a board requiring `xtest`, then `xtest` will run automatically.

Related Resources

The following related resources may prove necessary or helpful for your applications.

EDT Document	URL
EDT Application Programming Interface (API)	www.edt.com/api (HTML)
	www.edt.com/manuals/misc/api.pdf (PDF)
User's guide for EDT main boards	www.edt.com/manuals/PCD/pciss_gs.pdf
User's guides for EDT mezzanine boards	www.edt.com/manuals.html
User's guide for EDT CD/CDa boards	www.edt.com/manuals/PCD/pcicd.pdf

Using sslooptest

Use `sslooptest` to test the EDT boards indicated in Table 1.

Running `sslooptest` will determine the board configuration, load the appropriate test FPGA configuration file, generate loopback test data, and then test the board and its components.

The test is designed to verify that the board is installed properly and operating correctly.

NOTE Running `sslooptest` overwrites the configuration file in the user interface (UI) FPGA, so after the test is done, you'll need to reconfigure the board with `initpcd` (or your own application) to disable loopback.

To perform this test:

1. Install your board in the host computer, using your EDT installation package.
2. Disconnect any external cabling from the board.
3. At the command prompt, enter...

   `pciload`

   ...to display each board and its unit number; then enter...

   `sslooptest -u unit_number`

   ...replacing *`unit_number`* with the unit number.
4. Review the resulting output, which varies by product. For a functional board, the output will contain such lines as...

   `Total errs=0 bufs=4000; Channel errs(NNNNNNNNNNNNNNNx) bufs(YYYYYYYYYYYYYYYx)`

NOTE The number of `Y`, `N`, or `x` characters in parentheses reflects the number of DMA channels available on the board.

The string `Total errs...bufs` tells the following...

— After `errs` – the number shown is the total number of errors so far.

— After `bufs` – the number shown is the total number of buffers tested.

The string `Channel errs...bufs` tells the status of each channel. Inside each set of parentheses, the first character correlates to channel 0, the second to channel 1, and so on.

— After `errs – Y` means yes (i.e., an error is present on the channel); `N` means no (i.e., an error is not present on the channel); and `x` means the channel is not in use.

— After `bufs – Y` means yes (the buffer is in use and DMA is occuring on the channel); `N` indicates no (the buffer is in use, but DMA is not occurring on the channel); and `x` means the channel is not in use.

5. After the test is finished, reconfigure the board using `initpcd` (or your own application) to disable loopback.
6. Reconnect any external cabling to the board.

Using xtest

Use `xtest` to test the EDT boards indicated in Table 1.

Running `xtest` will load the FPGA configuration file `xtest.bit`, and then test the board and its components.

The test is designed to verify that the board is installed properly and operating correctly.

NOTE Running `xtest` overwrites the configuration file in the user interface (UI) FPGA, so after the test is done, you'll need to reconfigure the board with `initpcd` (or your own application) to disable loopback.

To perform this test:

1. Install your board in the host computer, using your EDT installation package.
2. Disconnect any external cabling from the board.
3. At the command prompt, enter...

   ```
   pciload
   ```

   ...to display each board and its unit number; then enter...

   ```
   xtest -u unit_number -a 1024
   ```

   ...replacing *`unit_number`* with the unit number.
4. Review the resulting output, which should resemble the following...

   ```
   reading 4096 words
   buf at 820000
   testing dirreg at 4 4
   testing dirout at 8 8
   testing dirin at 8 c
   testing ctlout at a a
   testing ctlin at a e
   Calling DMA read 8192 at 820000
   return to do read:
   read returned length 8192
   Done.
   checking data
   4096 words 0 errors
   buf 0 820000
   buf 1 920000
   reading 100 buffers of 1048576 bytes from unit 0 with 2 bufs
   return to start: starting read at 820000
   starting read at 920000
   hit return to continue:
   counter0 4628 2362958141 counter1 4628 3122437420 freq 0 266230000
   dtime 759479279.000000 ticktime 266230000.000000
   time is 2.852719 sec
   36757077.671371 bytes/sec
   ..................................................................
   ```

   ...where errors are indicated by the string `ERROR` followed by an error message. If you do not see such a string in the output, then the test has completed satisfactorily.
5. After the test is finished, reconfigure the board using `initpcd` (or your own application) to disable loopback.
6. Reconnect any external cabling to the board.

Revision Log

20130516 - Rev01 - by PH	Combined both older guides into this new guide, *Testing Procedures for sslooptest and xtest* (retaining the document number from the original *Testing Procedure: sslooptest*, Doc. #008-02780).
20070000 - by SV or LW	Created two test procedure guides: *Testing Procedure: sslooptest* (Doc. #008-02780) and*Testing Procedure: xtest* (Doc. #008-02779).